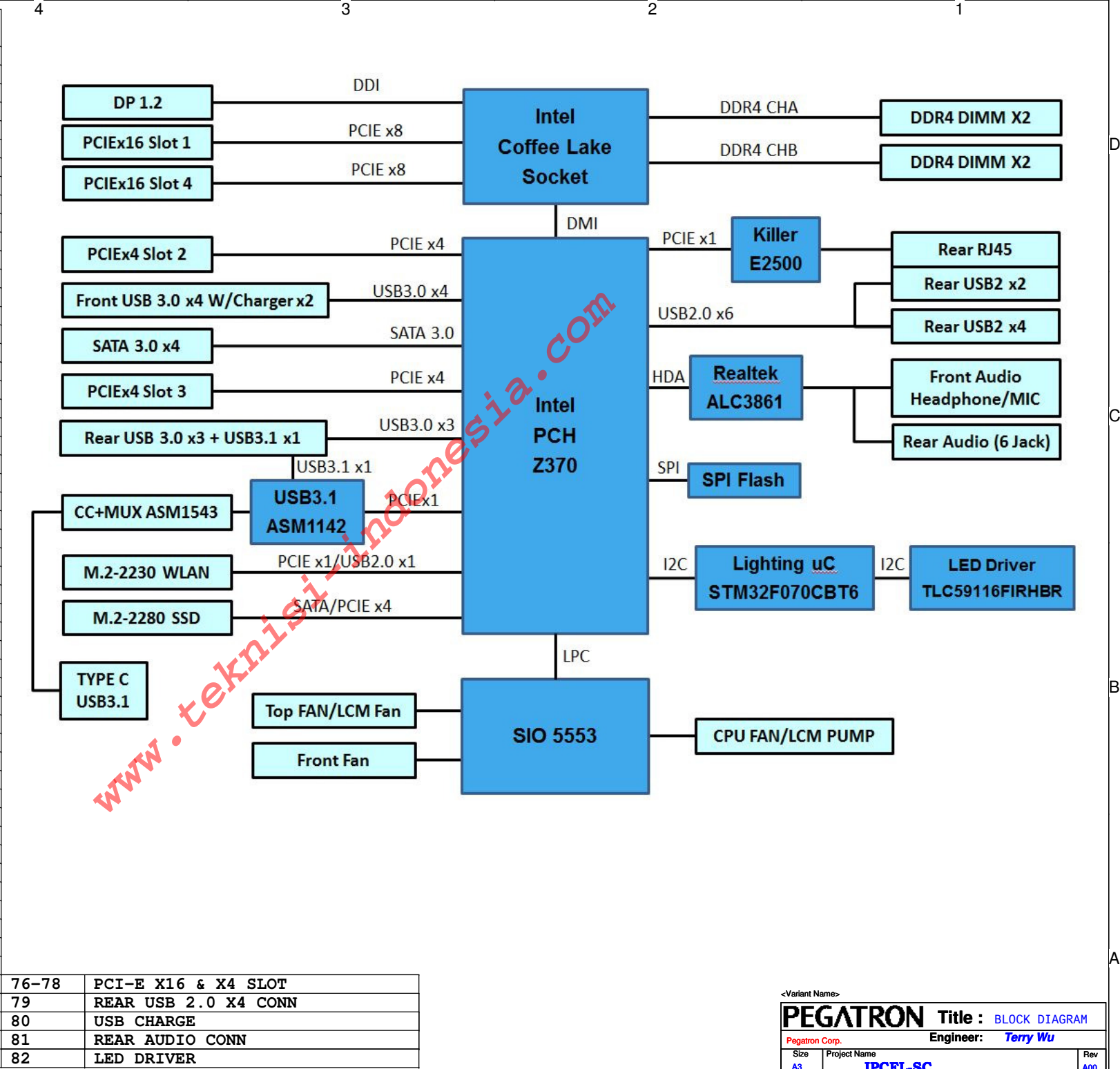


IPCFL-SC<sup>5</sup> Revision: A00

PAGE	TITLE
01	BLOCK DIAGRAM
02	CHANGE HISTORY
03	POWER FLOW
04	CLOCK DISTRIBUTION
05	POWER SEQUENCE
06	POWER DISTRIBUTION
07~12	CPU
13~17	DDR4
18~25	PCH
26	ME_Disable
27	RTC/CMOS/INTRUDER
28	SPI ROM
29	XDP
30	PWRBTN/RSTBTN
31	M.2 KEY A WLAN
32	M.2 KEY M SSD
33	PCI-E X16 SLOT1
34	AUDIO CODEC ALC3861-CG
35	FRONT AUDIO HEADER
36	ASM1142
37	ASM1543
38	XXXX
39	REAR TYPE C CONN
40	LAN_E2500
41	RJ45+USB2.0X2 CONN
42	REAR USB3.0X4 CONN
43	FRONT USB3.0 x 2 CONN -1
44	FRONT USB3.0 x 2 CONN -2
45	SATA CONN x 4
46	DP DONGLE CONTROL
47	DISPLAY PORT
48	SIO SCH5553-UH
49	LPC DEBUG HEADER
50	HDD/SSD_LED
51	LED FOR DEBUG
52-53	+5VSB/+3VSB/+3VA
54	+1VSB
55	+5V_1VSB_IN & +5V_DUAL
56	+1P2V/+1P2V_SUS/+3.3V_SUS
57	+1V_ST
58	VCORE & VGT
59	+1P2V_DAU1
60	+0P95V_CPU10
61	ATX POWER 24P CONN
62	+1P05V_SA
63-67	VCORE & VGT
68	VTT_DDR
69	MAIN POWER DISCHARGE
70	XXXX
71	FAN CIRCUIT/LIQUID PUMP
72	XXXX
73	SCREW HOLE
74	GFX_PWR
75	Lighting Micro-Controller



Schematics Change History

Version	Date	Page	Comments
X00	2017/05/17	75	Add uC Lighting micro-controller
X00	2017/05/17	7-12	Change CPU form KBL to CFL
X00	2017/05/17	39,42,43,44	Add AC caps for USB3.0/3.1 RX
X00	2017/05/17	39,42,43,44	Add common mode choke for USB3.0/3.1 TX form RF request
X00	2017/05/17	40	Change LoM from E2400 to E2500
X00	2017/05/17	48,73,75	Add Chassis Intrusion function
X00	2017/05/17	71	Add U.2 Blower
X00	2017/05/17	43, 44	Change front IO Power Cap from 2.2uF x2 to 100uF
X00	2017/05/17	43	Change USB3.0 header (P24) pin define for optimizing cable routing
X00	2017/06/26	39	Change Type-C CMC from 90 ohm to 67 ohm
A00	2017/07/20	31, 32, 42	Follow DFM rule, AC39, M2C14, M2C17, M2C2, M2C20, M2C5, O2CB10, O2CB11, O2CB16, O2CB2, O2CB7, O2CB8, UCB23 are changed from 0201 to 0402.
A00	2017/07/20	19	Update Board ID, install SR7698, SR712 and remove R545, SR7696.
A00	2017/07/20	77	Install SR7682, SR7683 for TBT3 card.
A00	2017/07/20	42, 43, 44	UC981, UC982, UC983, UC984, UC985, UC986, UC987, UC988, UC993, UC994, UC995, UC996 are changed to 330nF/10V for DELL recommend.
A00	2017/07/20	39, 43	UC975, UC976, UC977, UC978, UC979, UC980 are changed to 0 ohm for DELL recommend
A00	2017/07/20	71	Change pin define for blower device (KSB05105HC76J)
A00	2017/07/20	75	Follow ARD define to remove this feature
A00	2017/07/20	80	UR69742, UR69741, UR69744, UR69746, MQ34, MQ36, UR69743, UR69745 are removed to fix BITs BITS336329
A00	2017/07/20	20, 48	Follow EMC team requirement, SC141, SC147: 20pF/50V; SCB68: 47pF/50V
A00	2017/07/20	35	Follow codec vendor requirement, AR5, AR6 are changed from 1K ohn to 75 hm.
A00	2017/07/24	10, 20, 23, 28, 33, 40, 41, 76, 77, 78, 79	XR15, CR17, F3R14, F3R20, F3R21, F3R7, F3R8, HR17, HR18, LR20, LR22, M2R40, SR4, SR44, SR747, SR80, SR81, SR82, SR85, M2R41, XR11, M2R43, M2R44 are changed from 0 ohm to short pin.

<Variant Name>

Pegatron Corp.

Size  
A2

Project Name  
IPCFL-SC

Date: Monday, July 24, 2017

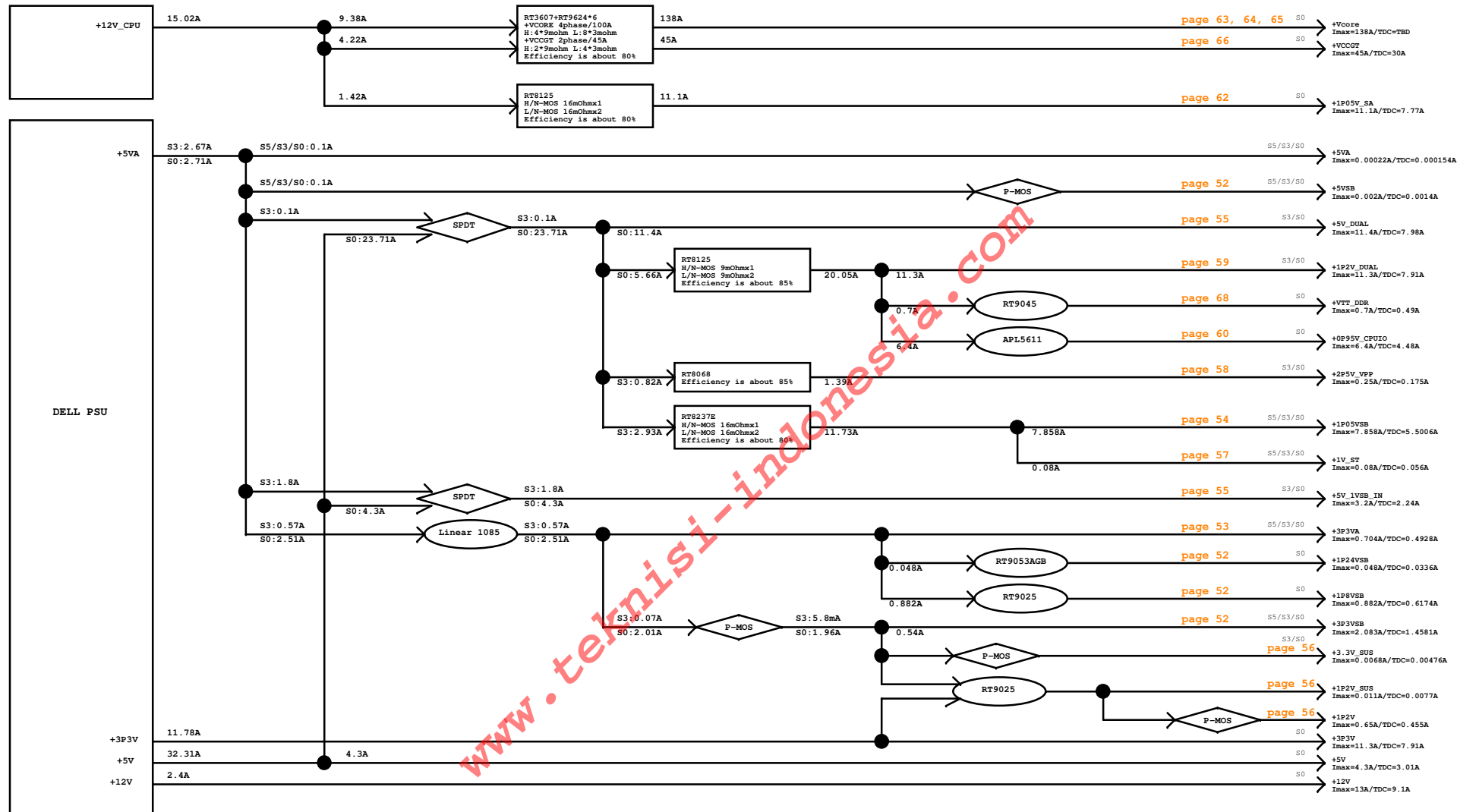
Engineer: Terry Wu

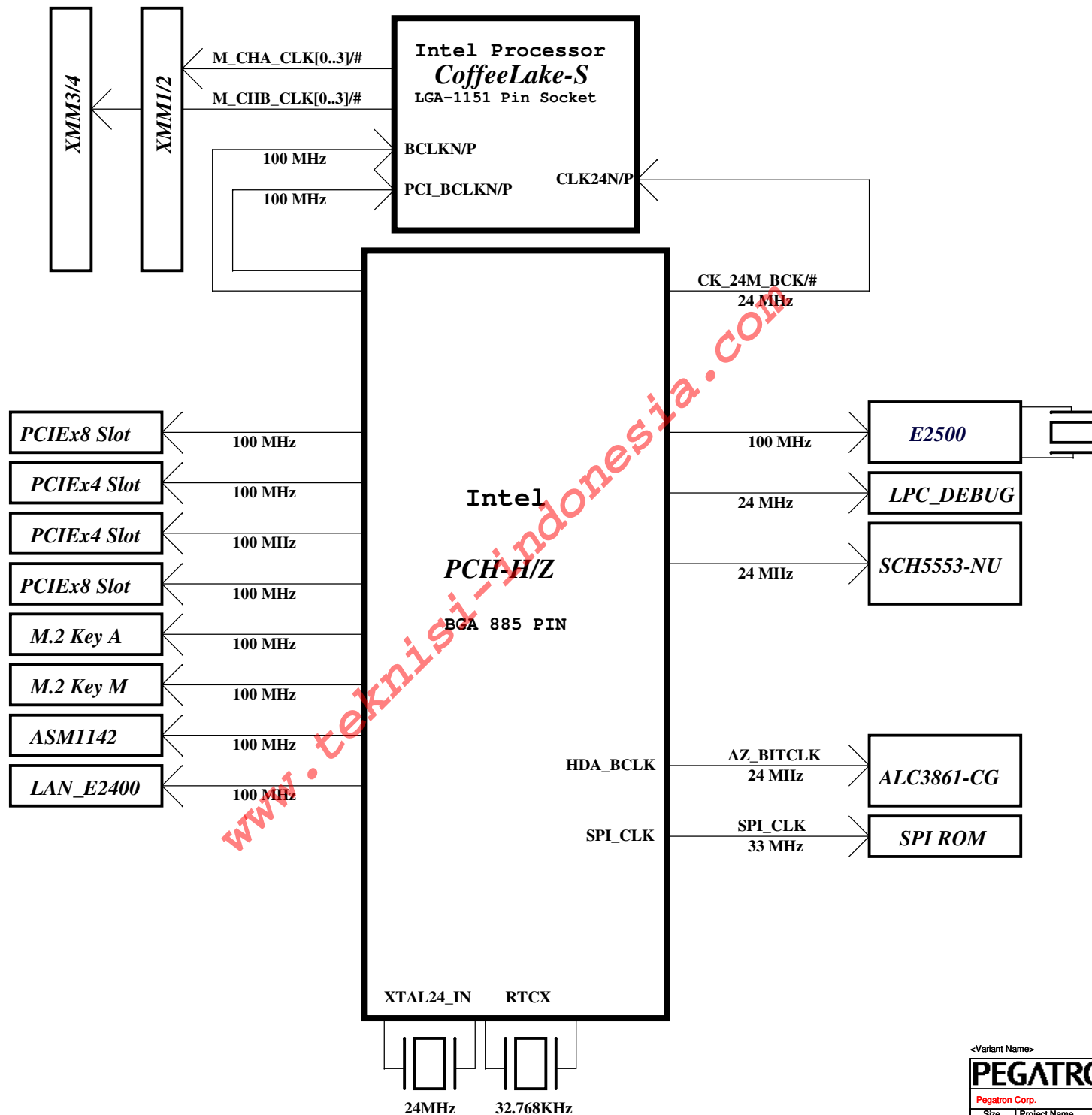
Rev  
A00

Sheet 2 of 82

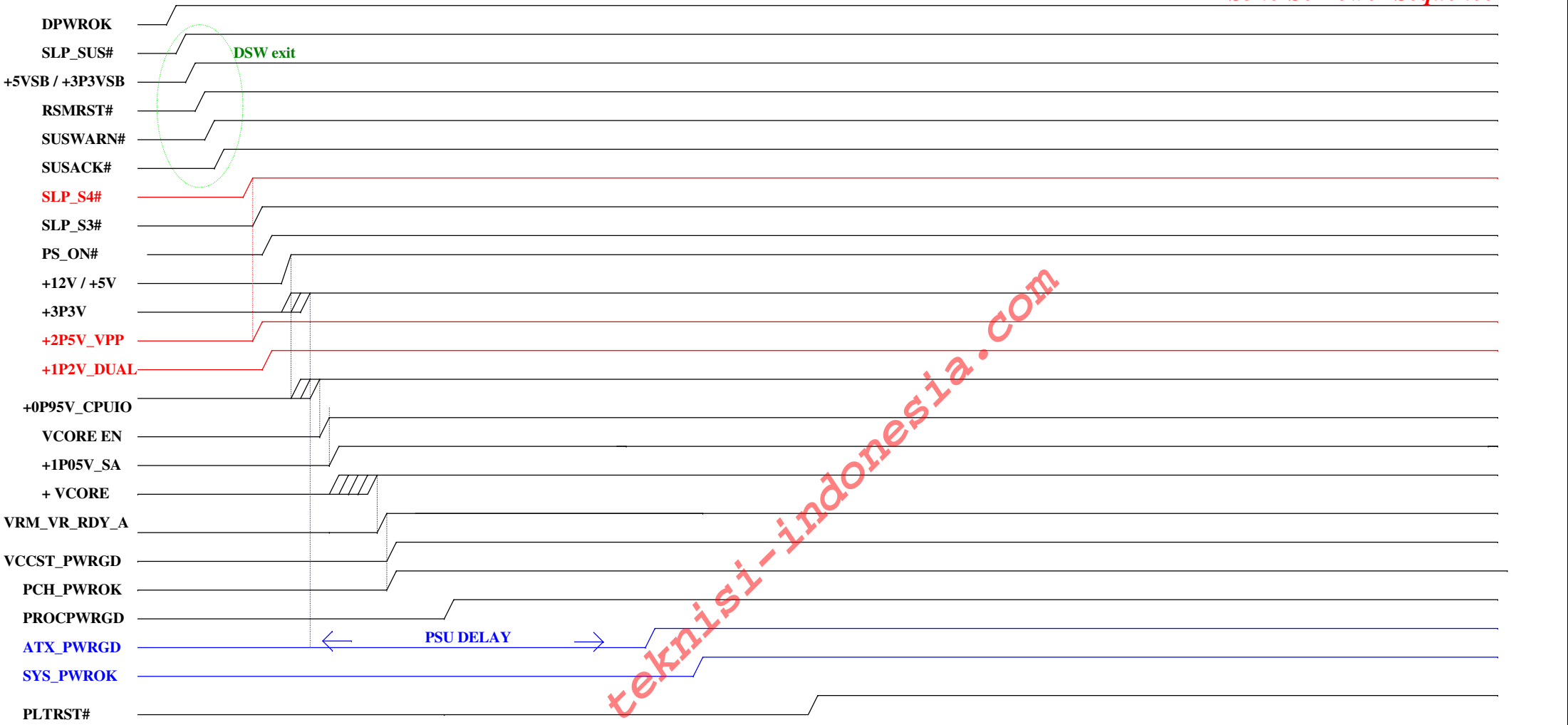
1

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S5 to S0 Power Sequence



	<b>CPU CaffeLake-S 65W/95W</b>
+VCORE	-> 138A (Imax)
+0P95V_CPUIO	-> 6.4A (Imax)
+1P05V_SA	-> 11.1A (Imax)
+V_AXG	-> 45A (Imax)

	<b>PCH Z370</b>
+1VSB	-> 7.858A
+3P3V	-> 0.007A
+3P3VSB	-> 0.78A
+3P3VA	-> 0.20A
+BATT	RTC(G3) -> 6uA

	<b>DDR4-2667(4) &amp; Termination</b>
+1P2V_DUAL	-> 8A
+VPP(2.5V)	-> 0.25A
+VTT_DDR(0.75V)	-> 0.7A

	<b>PCI Express x 16 (75W)</b>
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

	<b>PCI Express x 4 (25W)</b>
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	<b>PCI Express x 4 (25W)</b>
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	<b>PCI Express x 16 (75W)</b>
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

+5V_DUAL	<b>REAR USB2.0 6 PORTS</b>
	->3A

+5V_DUAL	<b>REAR USB3.0 4 PORTS</b>
	->3.6A

+3P3V	<b>M.2 SSD / M.2 WIFI</b>
	-> 0.9A / 0.6A

+3P3VSB	<b>Killer E2500</b>
	-> 0.151A

+5V_DUAL	<b>REAR TYPE C</b>
	->3A

+12V_CPU	<b>TOP FAN</b>
	-> 0.8A

+12V_CPU	<b>PUMP/CPU FAN</b>
	-> 0.208A / 0.7A

+12V_CPU	<b>GFX FAN</b>
	-> 0.8A

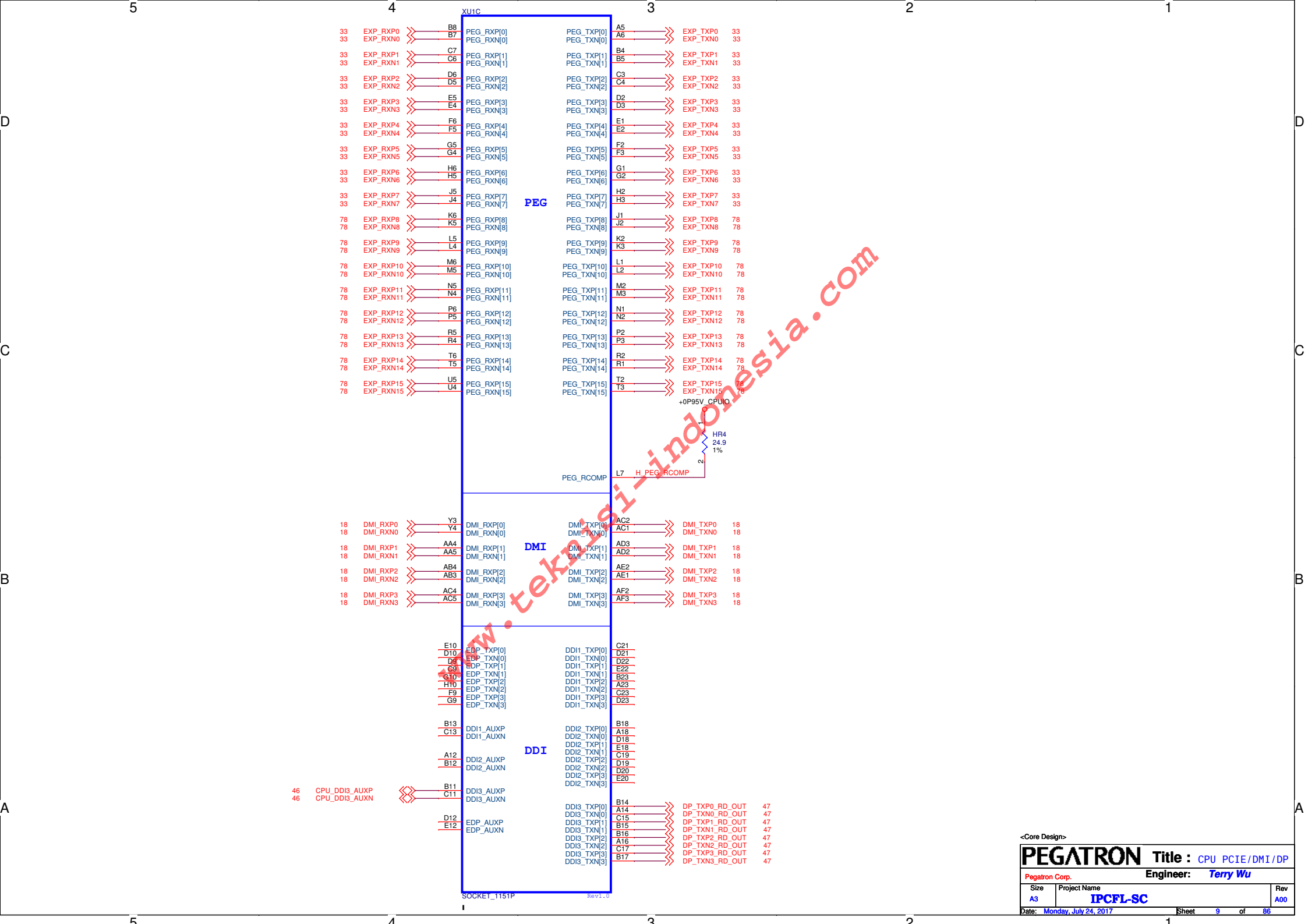
+5V_DUAL	<b>FRONT USB3.0 2 PORTS</b>
	->1.8A

+5V_1VSB_IN	<b>FRONT USB3.0 2 PORTS Charge</b>
	->3.2A









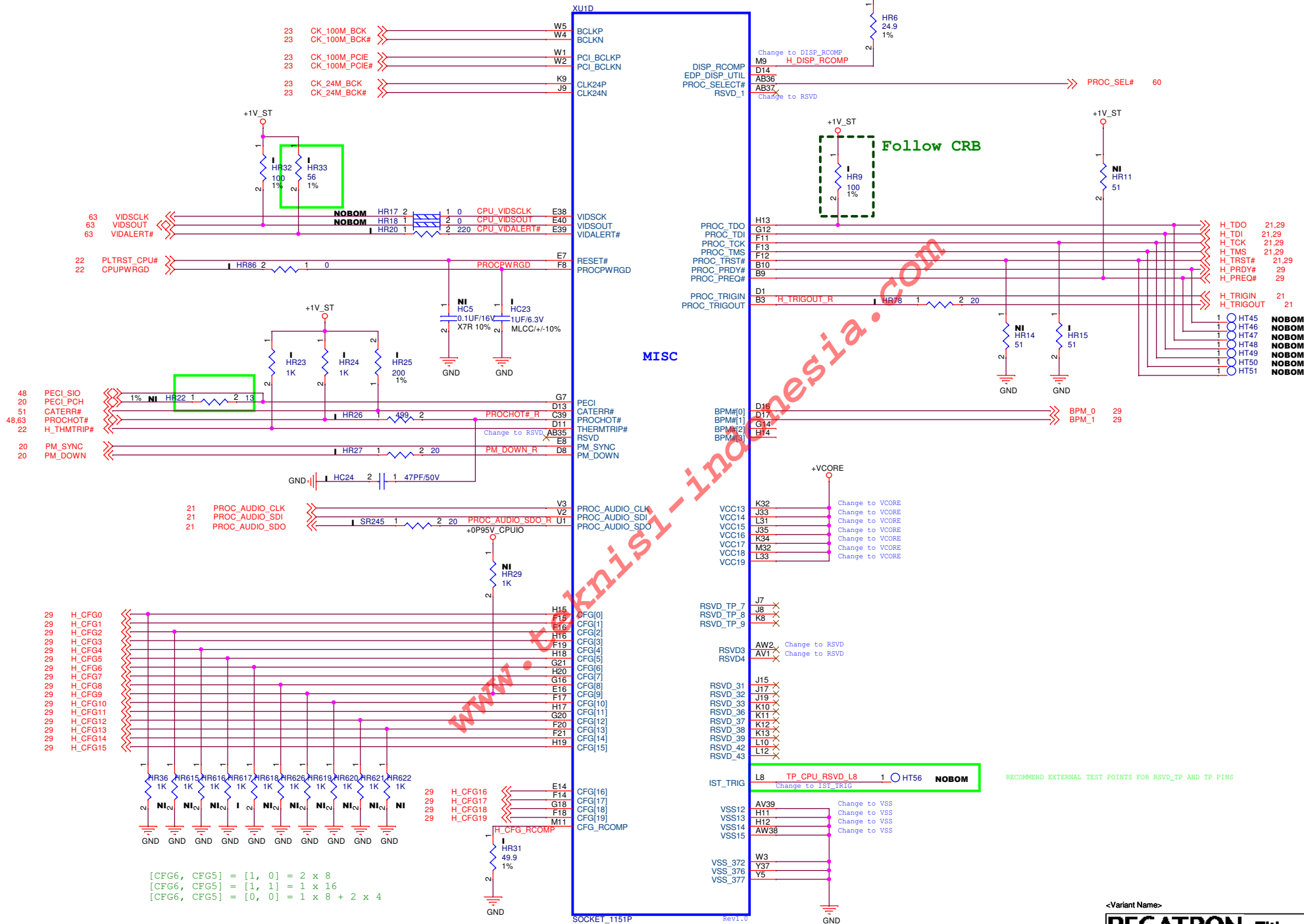
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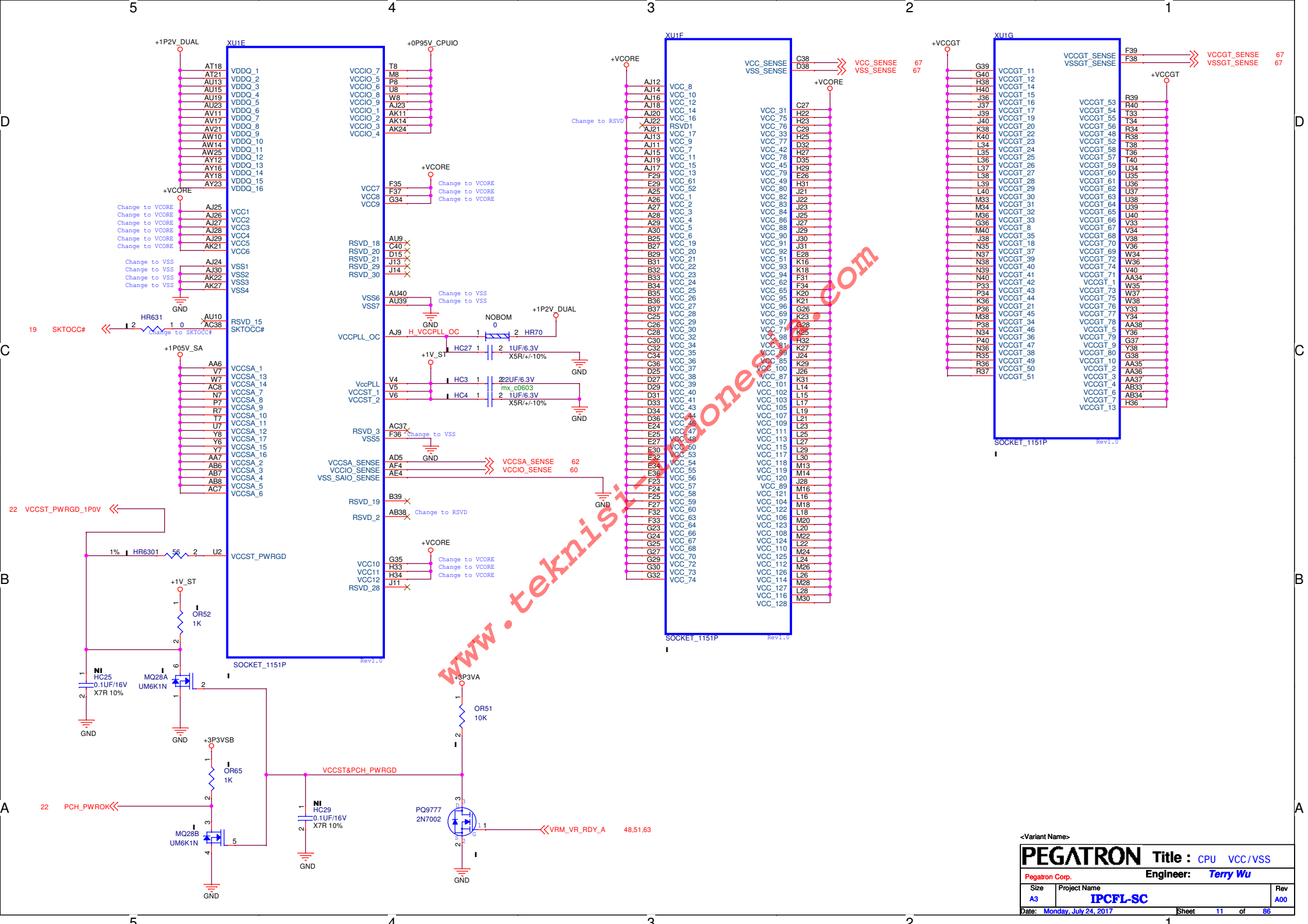
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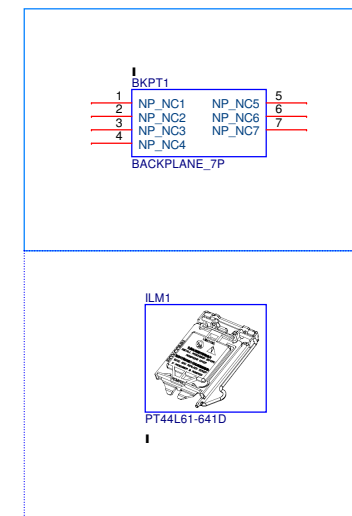
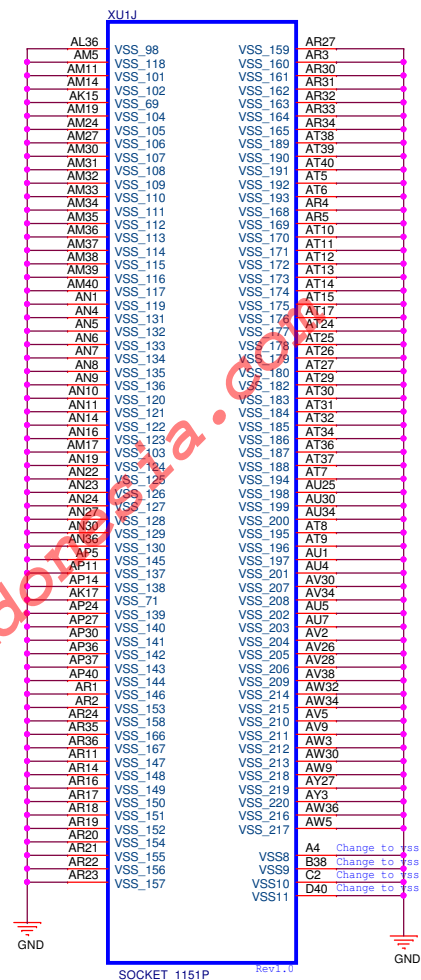
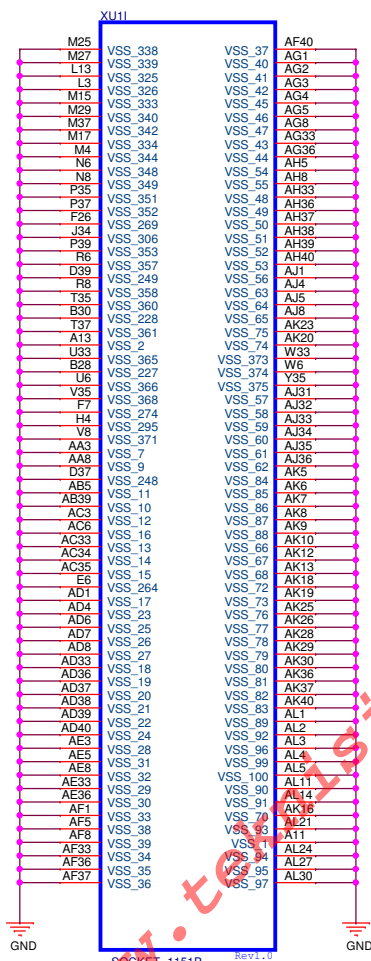
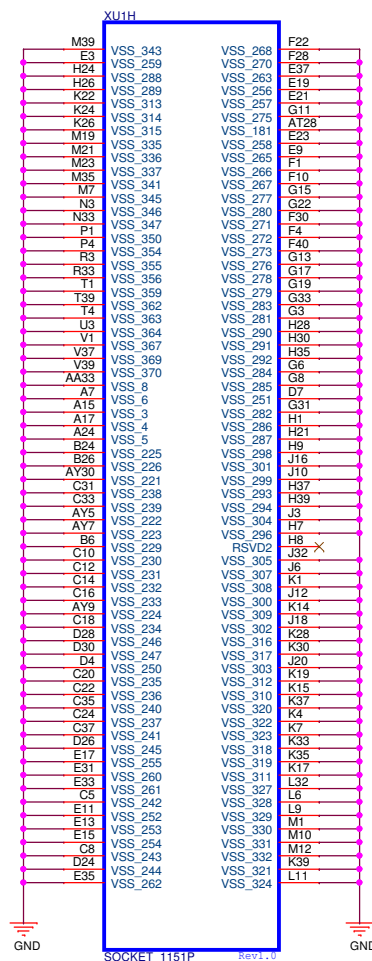
Pegatron Corp. Engineer: Terry Wu

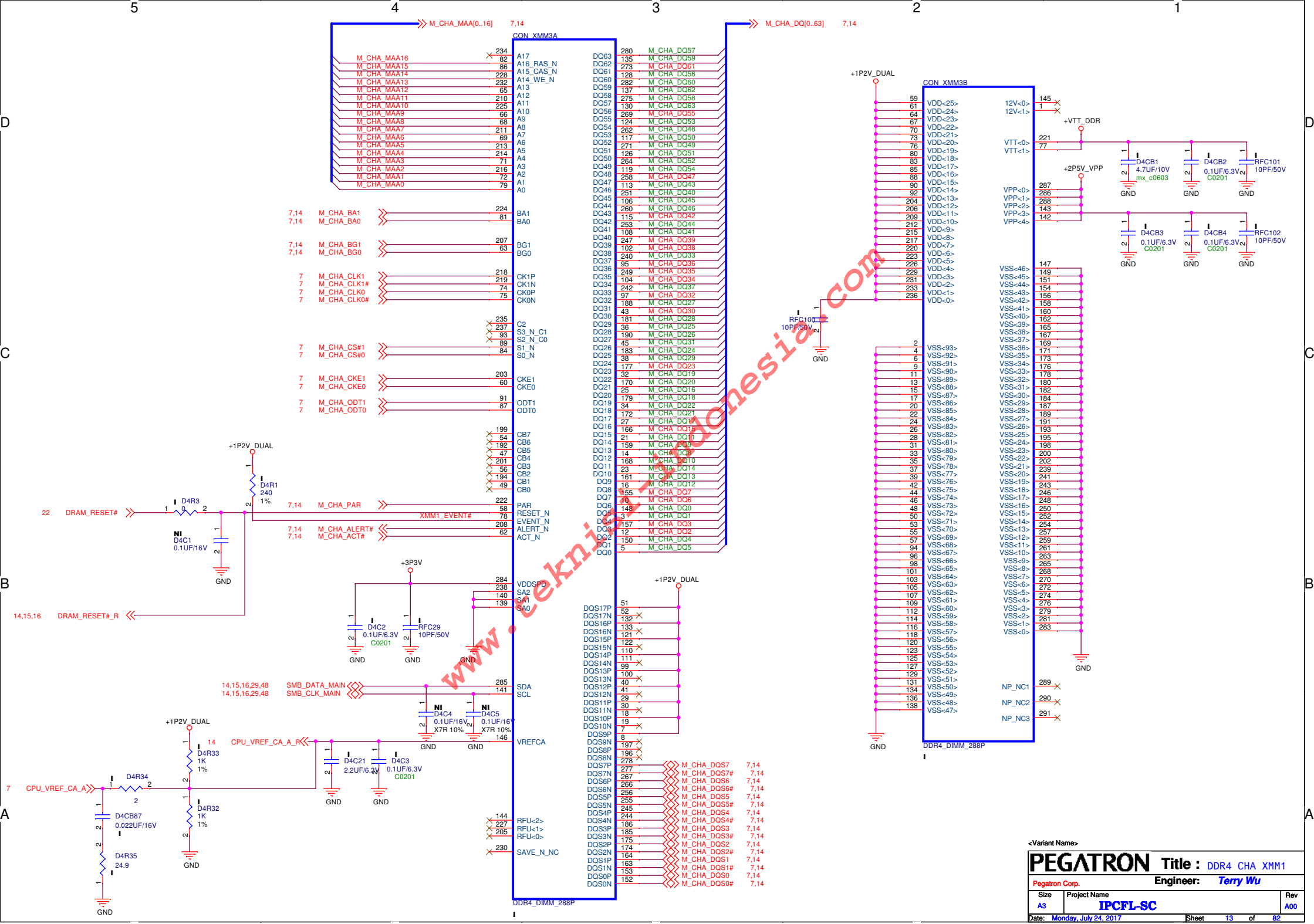
Size	Project Name	Rev
A3	IPCFL-SC	A00

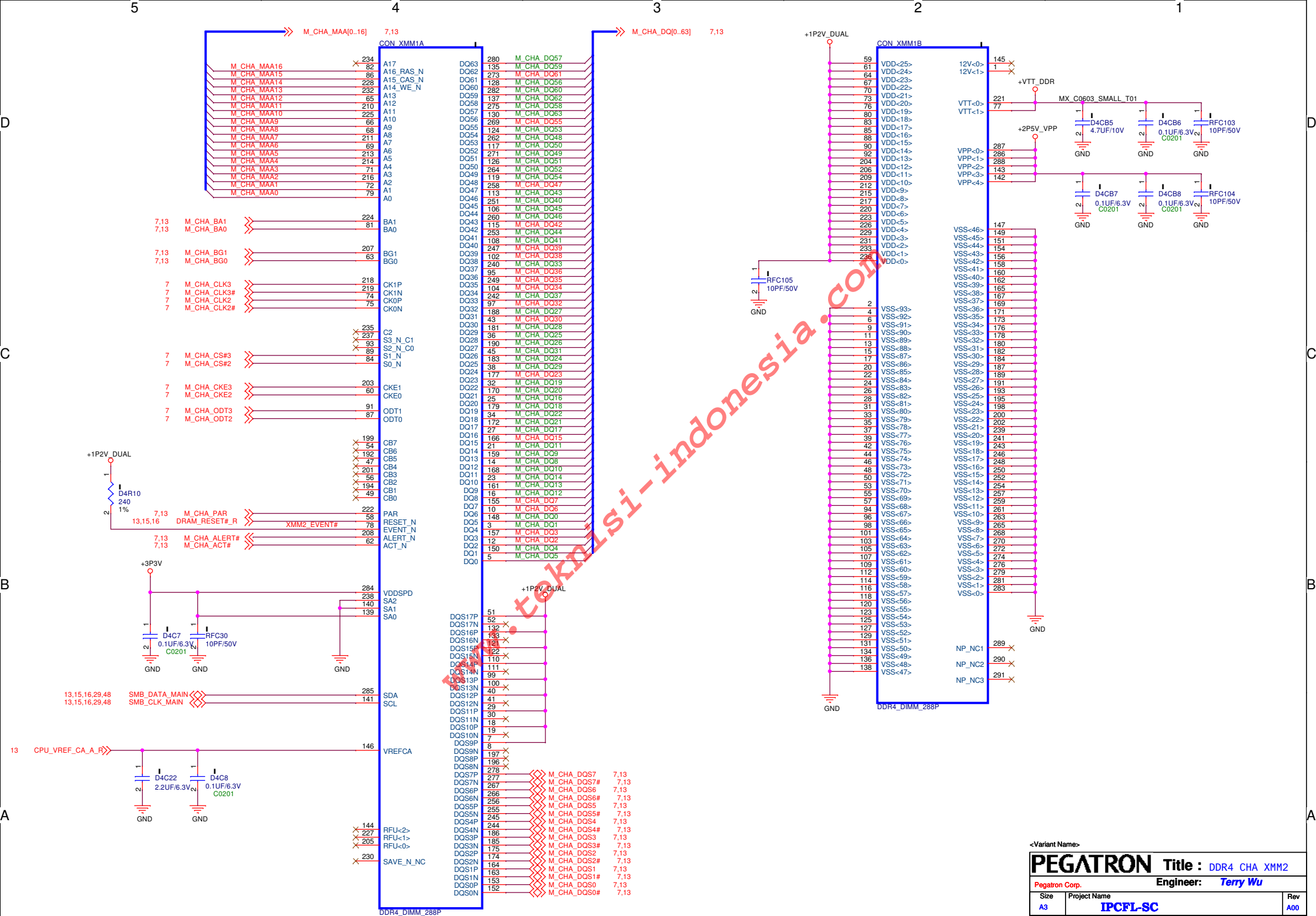
Date: Monday, July 24, 2017 Sheet 9 of 86



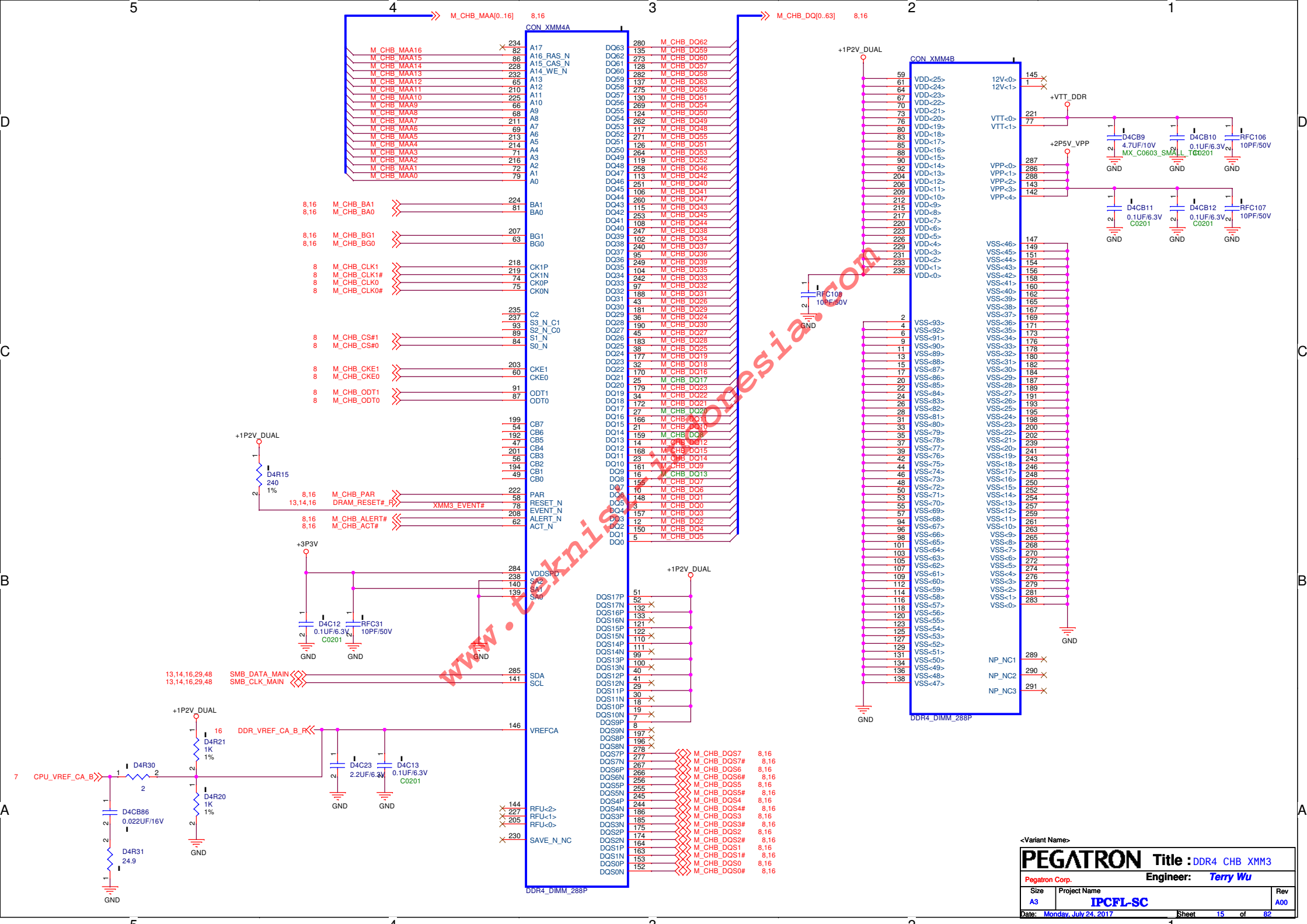


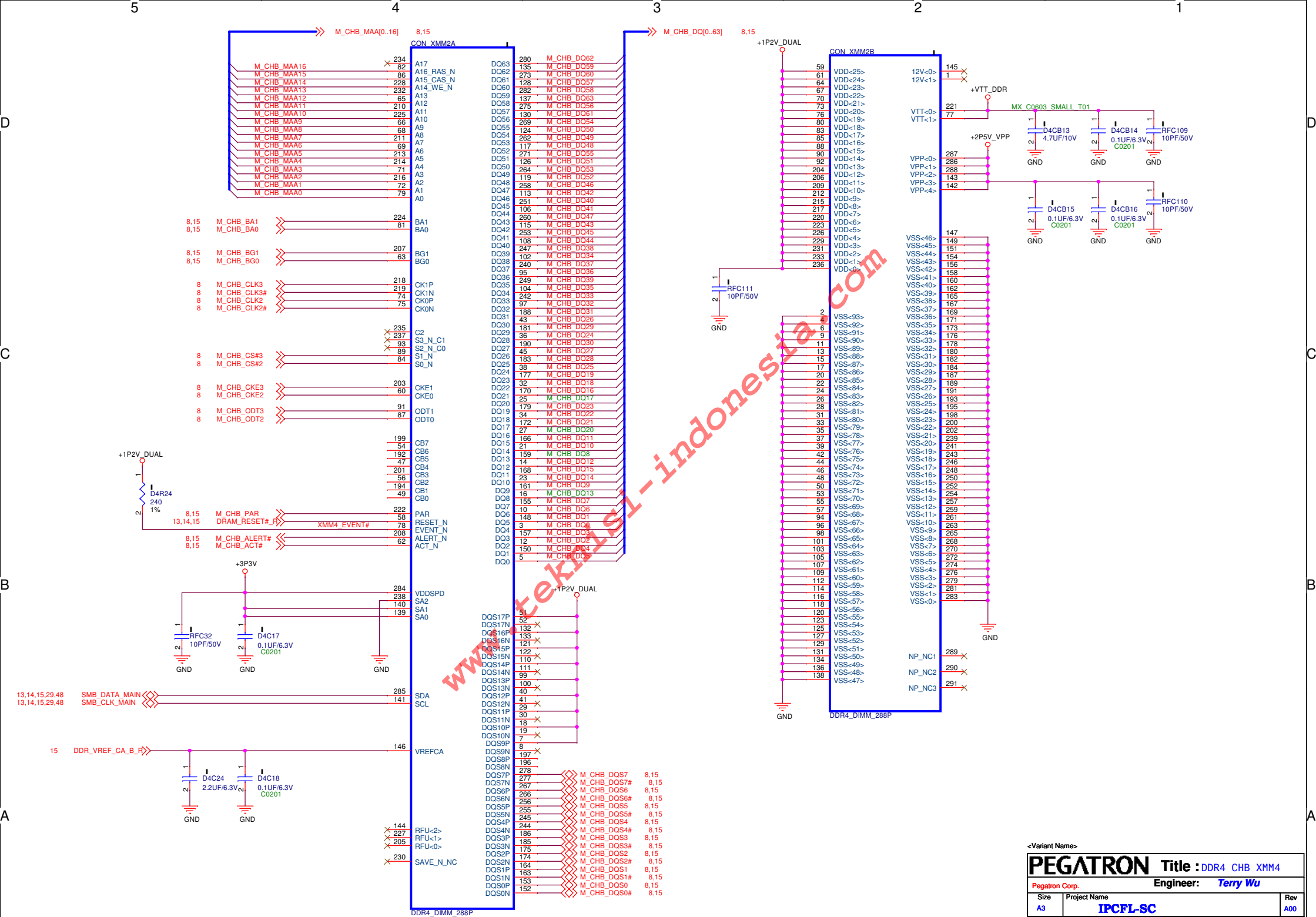






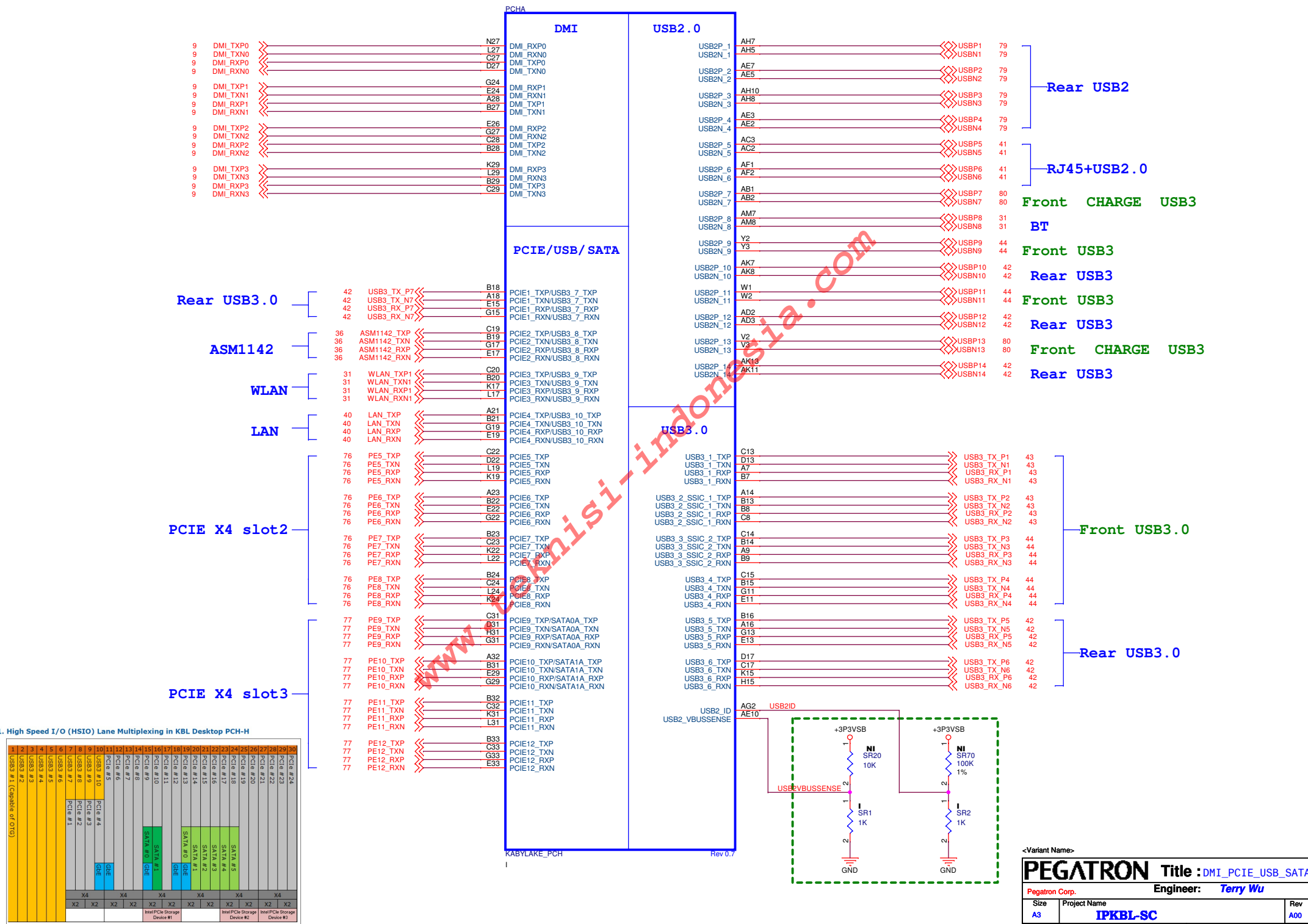












SATA HDD1

SATA HDD2

SATA HDD3

SATA HDD4

M.2 Key M slot

PCHB

### PCIE/SATA

B36  
C36  
E36  
G36  
PCIE13\_TXP/SATA0B\_TXP  
PCIE13\_TXN/SATA0B\_TXN  
PCIE13\_RXP/SATA0B\_RXP  
PCIE13\_RXN/SATA0B\_RXN

B37  
A37  
G37  
E37  
PCIE14\_TXP/SATA1B\_TXP  
PCIE14\_TXN/SATA1B\_TXN  
PCIE14\_RXP/SATA1B\_RXP  
PCIE14\_RXN/SATA1B\_RXN

B38  
C38  
C42  
E41  
PCIE15\_TXP/SATA2\_TXP  
PCIE15\_TXN/SATA2\_TXN  
PCIE15\_RXP/SATA2\_RXP  
PCIE15\_RXN/SATA2\_RXN

A39  
B39  
E43  
D42  
PCIE16\_TXP/SATA3\_TXP  
PCIE16\_TXN/SATA3\_TXN  
PCIE16\_RXP/SATA3\_RXP  
PCIE16\_RXN/SATA3\_RXN

F45  
E45  
K39  
J41  
PCIE17\_TXP/SATA4\_TXP  
PCIE17\_TXN/SATA4\_TXN  
PCIE17\_RXP/SATA4\_RXP  
PCIE17\_RXN/SATA4\_RXN

G44  
G45  
M41  
M39  
PCIE18\_TXP/SATA5\_TXP  
PCIE18\_TXN/SATA5\_TXN  
PCIE18\_RXP/SATA5\_RXP  
PCIE18\_RXN/SATA5\_RXN

H45  
H44  
P41  
P39  
PCIE19\_TXP/SATA6\_TXP  
PCIE19\_TXN/SATA6\_TXN  
PCIE19\_RXP/SATA6\_RXP  
PCIE19\_RXN/SATA6\_RXN

J44  
J43  
P36  
P38  
PCIE20\_TXP/SATA7\_TXP  
PCIE20\_TXN/SATA7\_TXN  
PCIE20\_RXP/SATA7\_RXP  
PCIE20\_RXN/SATA7\_RXN

K44  
K43  
T41  
T39  
PCIE\_21\_TXP  
PCIE\_21\_TXN  
PCIE\_21\_RXP  
PCIE\_21\_RXN

L44  
L43  
V36  
V35  
PCIE\_22\_TXP  
PCIE\_22\_TXN  
PCIE\_22\_RXP  
PCIE\_22\_RXN

N45  
N44  
V41  
V39  
PCIE\_23\_TXP  
PCIE\_23\_TXN  
PCIE\_23\_RXP  
PCIE\_23\_RXN

P44  
P43  
Y41  
Y39  
PCIE\_24\_TXP  
PCIE\_24\_TXN  
PCIE\_24\_RXP  
PCIE\_24\_RXN

AF44  
AG41  
AH39  
AH36  
AF45  
GPP\_F9/DEVSLP3  
GPP\_F6/DEVSLP4  
GPP\_F7/DEVSLP5  
GPP\_F8/DEVSLP6  
GPP\_F9/DEVSLP7

AE30  
AH35  
AE44  
AE43  
AD44  
GPP\_F10/SCLOCK  
GPP\_F11/SLOAD  
GPP\_F12/SDATAOUT1  
GPP\_F13/SDATAOUT0  
GPP\_F14

AC42  
AE35  
AE36  
GPP\_F19/6DP\_VDDEN  
GPP\_F20/6DP\_BKLTEN  
GPP\_F21/6DP\_BKLTCTL

AB45  
AE39  
GPP\_F22  
GPP\_F23

GPP\_E0/SATAXPCIE0/SATAGP0  
GPP\_E1/SATAXPCIE1/SATAGP1  
GPP\_E2/SATAXPCIE2/SATAGP2

GPP\_E3/CPU\_GP0  
GPP\_E4/DEVSLP0  
GPP\_E5/DEVSLP1  
GPP\_E6/DEVSLP2  
GPP\_E7/CPU\_GP1  
GPP\_E8/SATALED#

GPP\_E9/USB\_OC0#  
GPP\_E10/USB\_OC1#  
GPP\_E11/USB\_OC2#  
GPP\_E12/USB\_OC3#

GPP\_F15/USB\_OCB4#  
GPP\_F16/USB\_OCB5#  
GPP\_F17/USB\_OCB6#  
GPP\_F18/USB\_OC7#

GPP\_I0/DDPB\_HPD0  
GPP\_I1/DDPC\_HPD1  
GPP\_I2/DDPD\_HPD2  
GPP\_I3/DDPE\_HPD3  
GPP\_I4/EDP\_HPD

GPP\_I5/DDPB\_CTRLCLK  
GPP\_I6/DDPB\_CTRLDATA  
GPP\_I7/DDPC\_CTRLCLK  
GPP\_I8/DDPC\_CTRLDATA  
GPP\_I9/DDPD\_CTRLCLK  
GPP\_I10/DDPD\_CTRLDATA

GPP\_F0/SATAXPCIE3/SATAGP3  
GPP\_F1/SATAXPCIE4/SATAGP4  
GPP\_F2/SATAXPCIE5/SATAGP5  
GPP\_F3/SATAXPCIE6/SATAGP6  
GPP\_F4/SATAXPCIE7/SATAGP7

AM36  
AM35  
AM34

AP41  
AL44  
AL45  
AK44  
AK43  
AJ44

AJ43  
AH44  
AM39  
AK42

AD43  
AC44  
AH42  
AC43

AP7  
AT8  
AP8  
AT7  
BA1

AW5  
AV7  
AT5  
BA6  
AY1  
AY2

AK36  
AK33  
AK38  
AH43  
AE42

+3P3V

SR94  
10K  
1%

NI  
FC8  
0.1UF/16V  
X7R 10%

GND

+3P3VSB

SR129  
10K

USB\_OC0#

USB\_OC1#

USB\_OC2#

USB\_OCB4#

USB\_OCB5#

OC\_ASM1142\_PA#

36,42

ASM1142\_SMI#

DDPD\_HPD

47

PCH\_DDPD\_CTRLCLK

PCH\_DDPD\_CTRLDATA

46

SATA2\_PCIE3\_DET

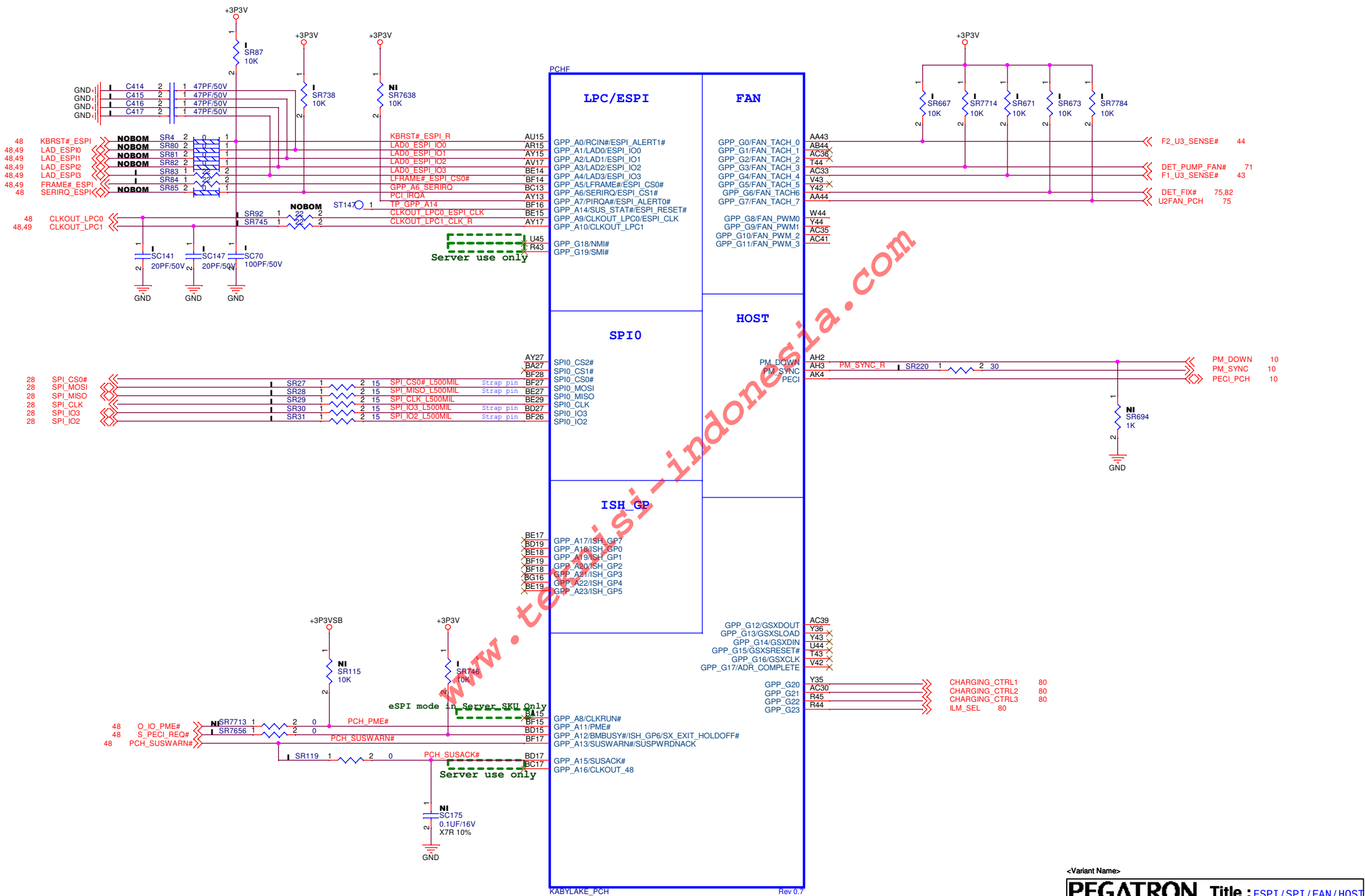
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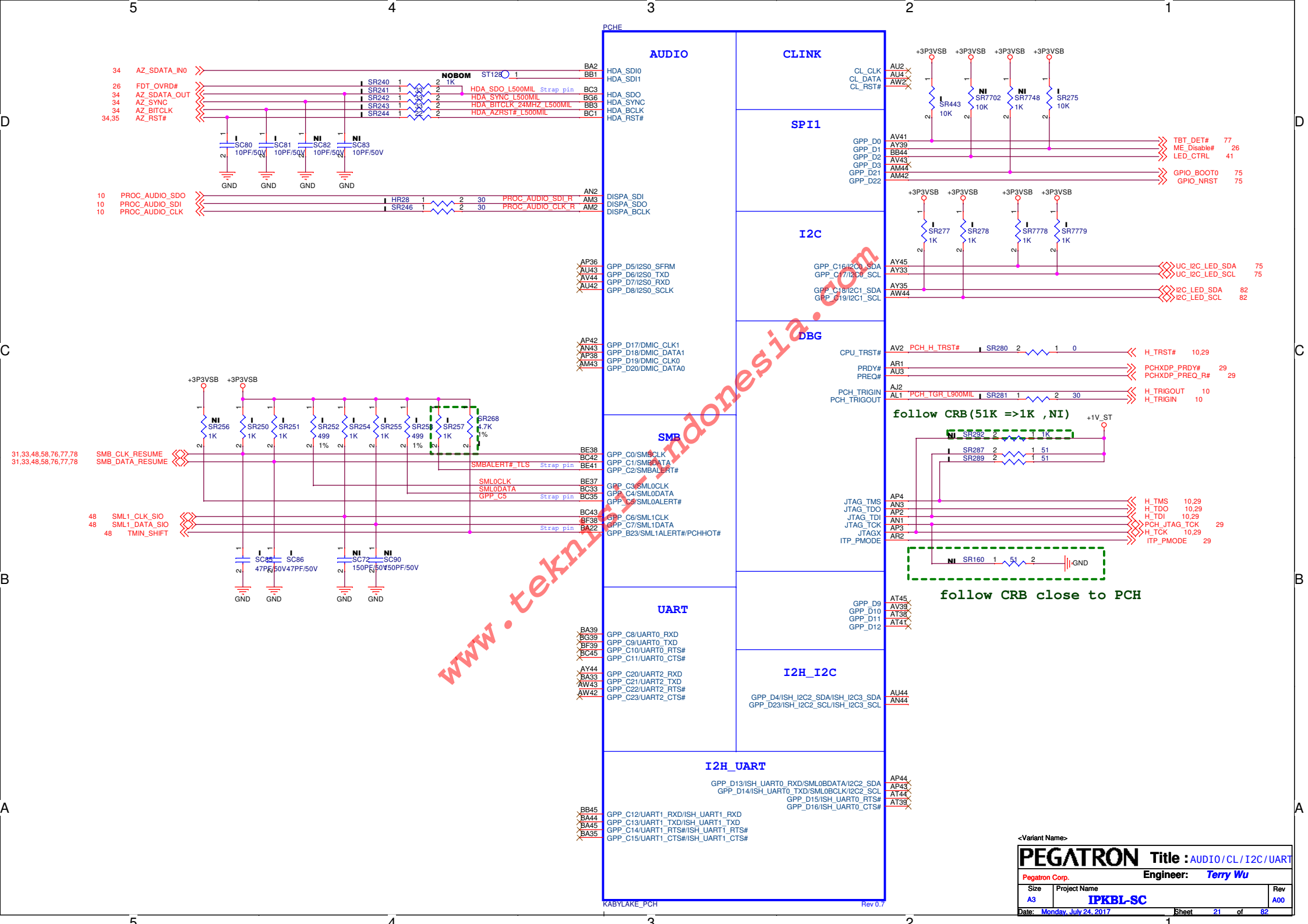
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USB_OC1#	U3_PORT2	U2_PORT13	+5V_Charger_2
USB_OC2#	U3_PORT3	U2_PORT9	+VCC_USB3_3
USB_OC3#	U3_PORT6	U2_PORT10	+VCC_USB3_2
USB_OCB4#	N/A	U2_PORT1	+VCC_USB2
USB_OCB5#	N/A	U2_PORT5	+VCC_USB2_1
USB_OC6#			

Version	Board_ID_D2	Board_ID_D1	Board_ID_D0
CFL_B00	0	0	0
CFL_X00	0	0	1
CFL_X01	0	1	0
CFL_X02	0	1	1
CFL_A00	1	0	0

<Variant Name>

PEGATRON		Title : SATA/PCIE	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name	Rev	
A3	IPKBL-SC	A00	
Date: Monday, July 24, 2017	Sheet	19	of 82





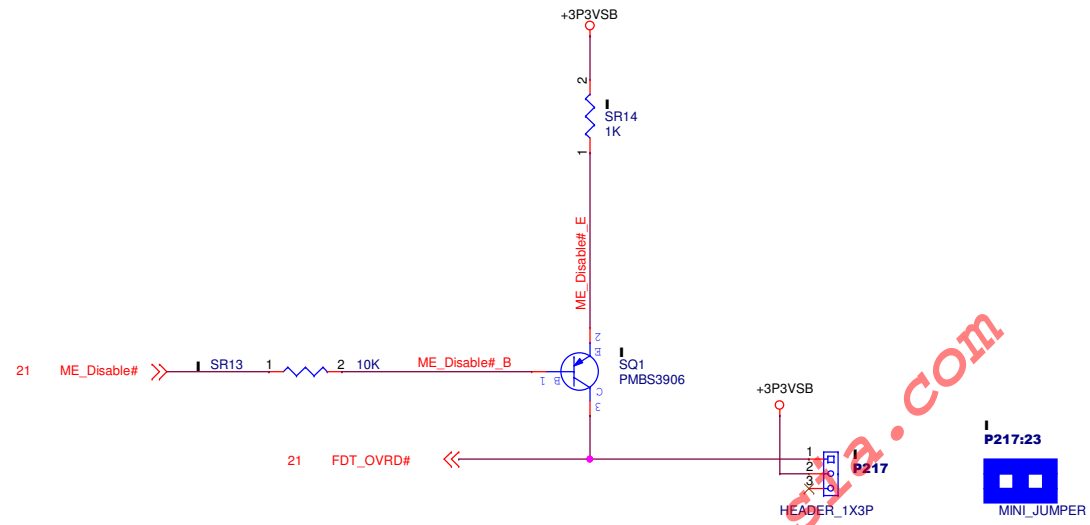






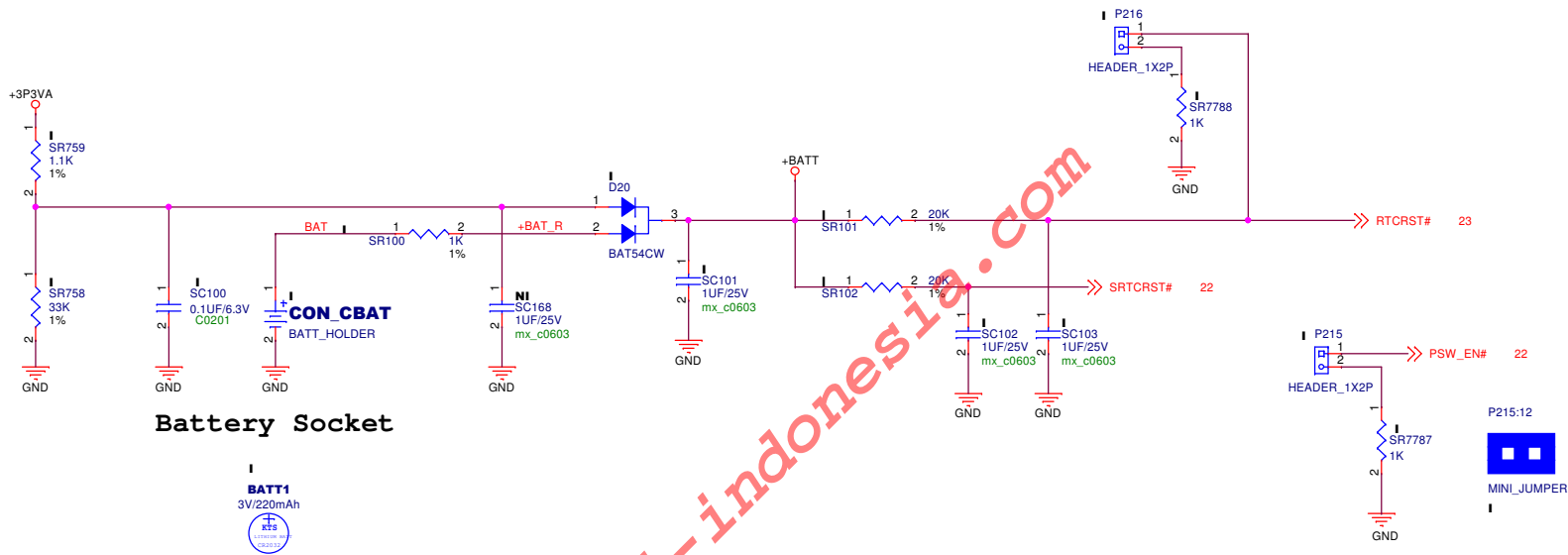




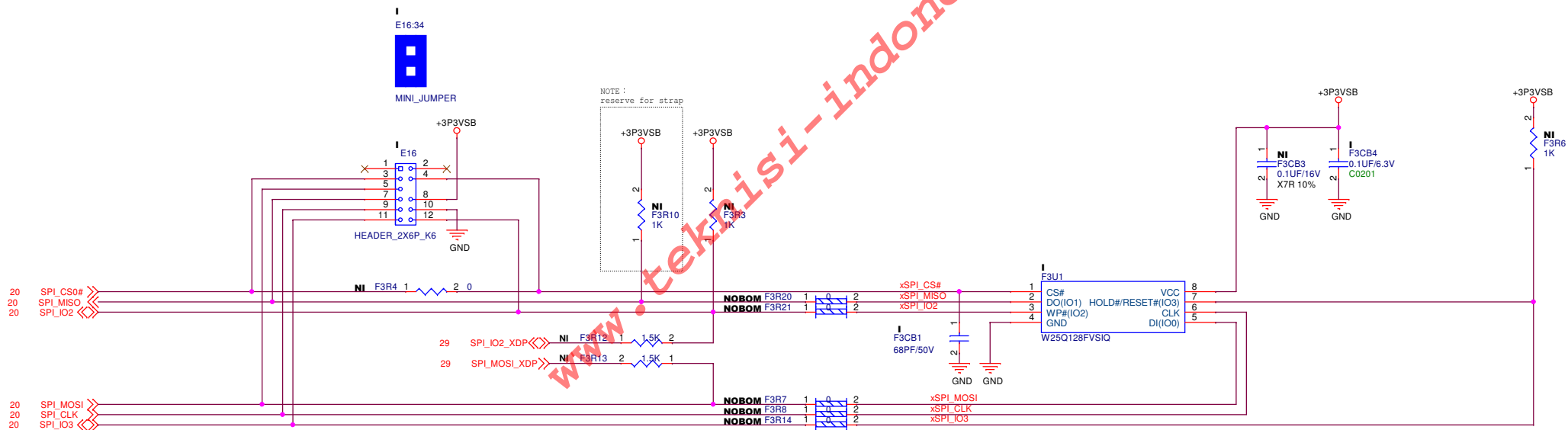


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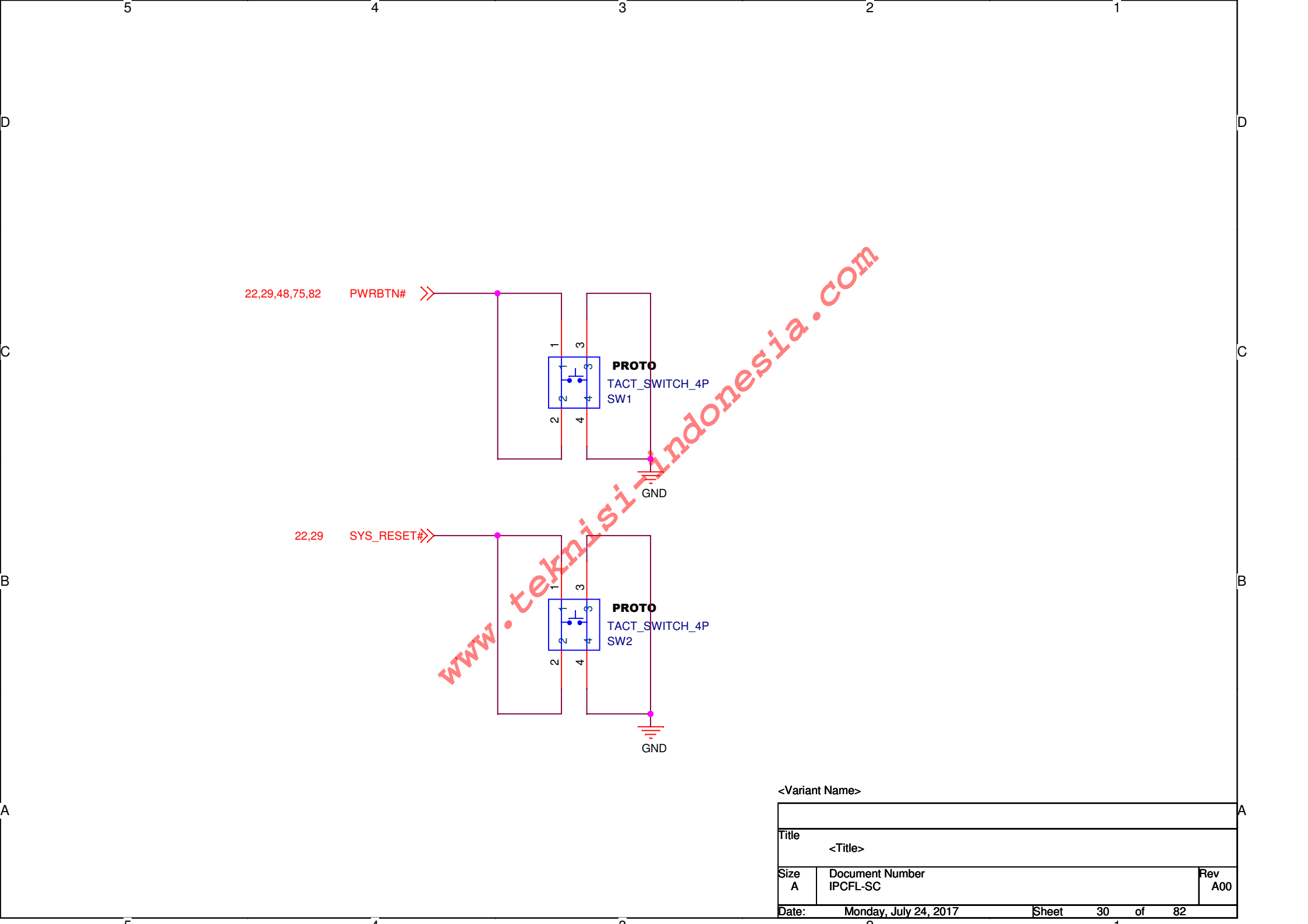
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Pegatron Corp.		Engineer: Terry Wu	
Size B	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet 26 of 82	

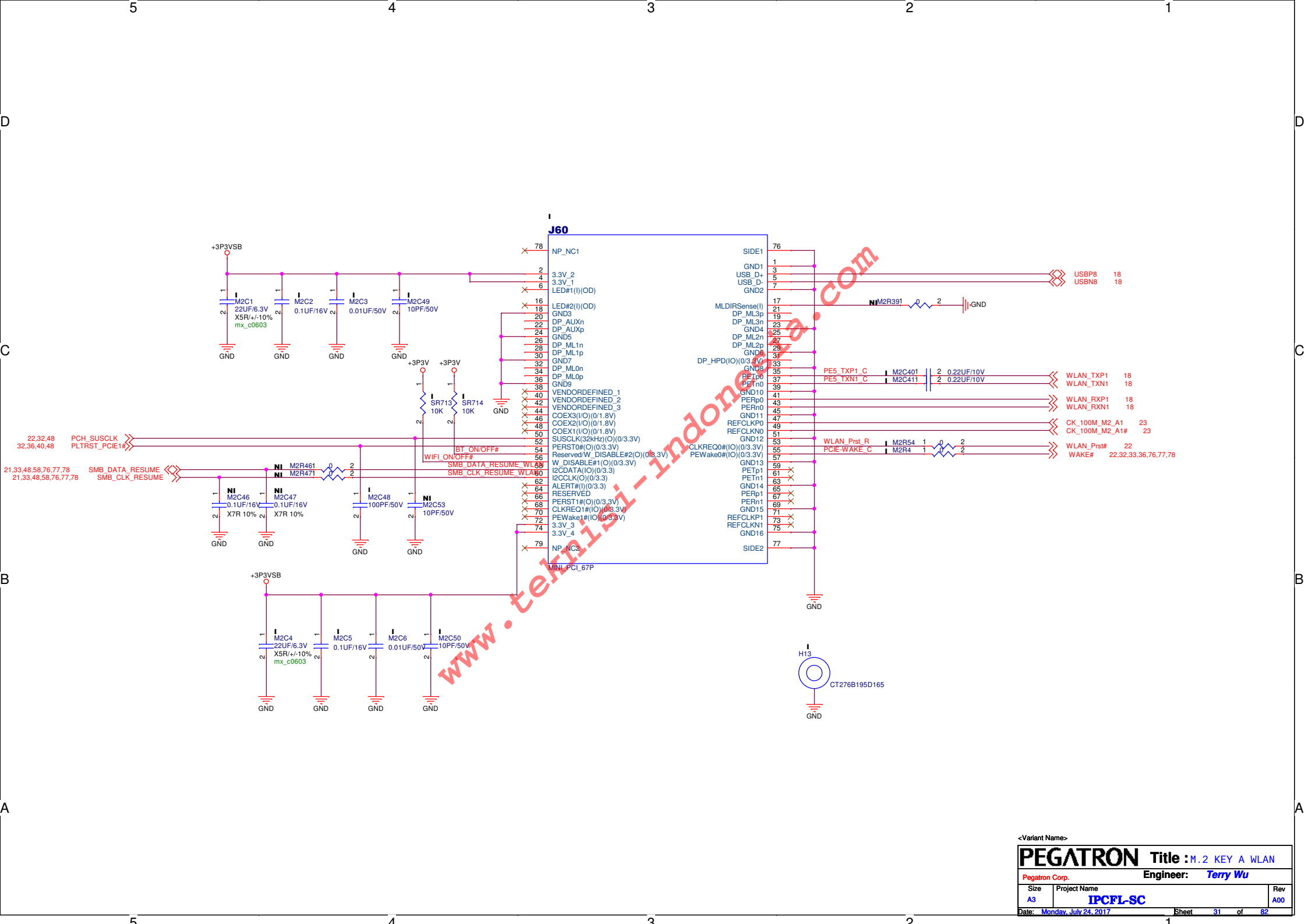


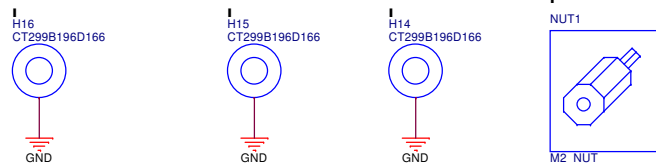
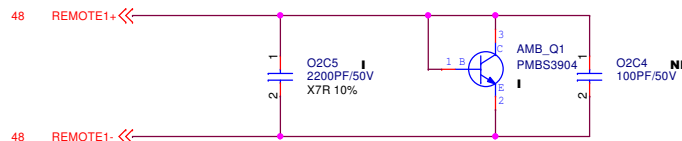
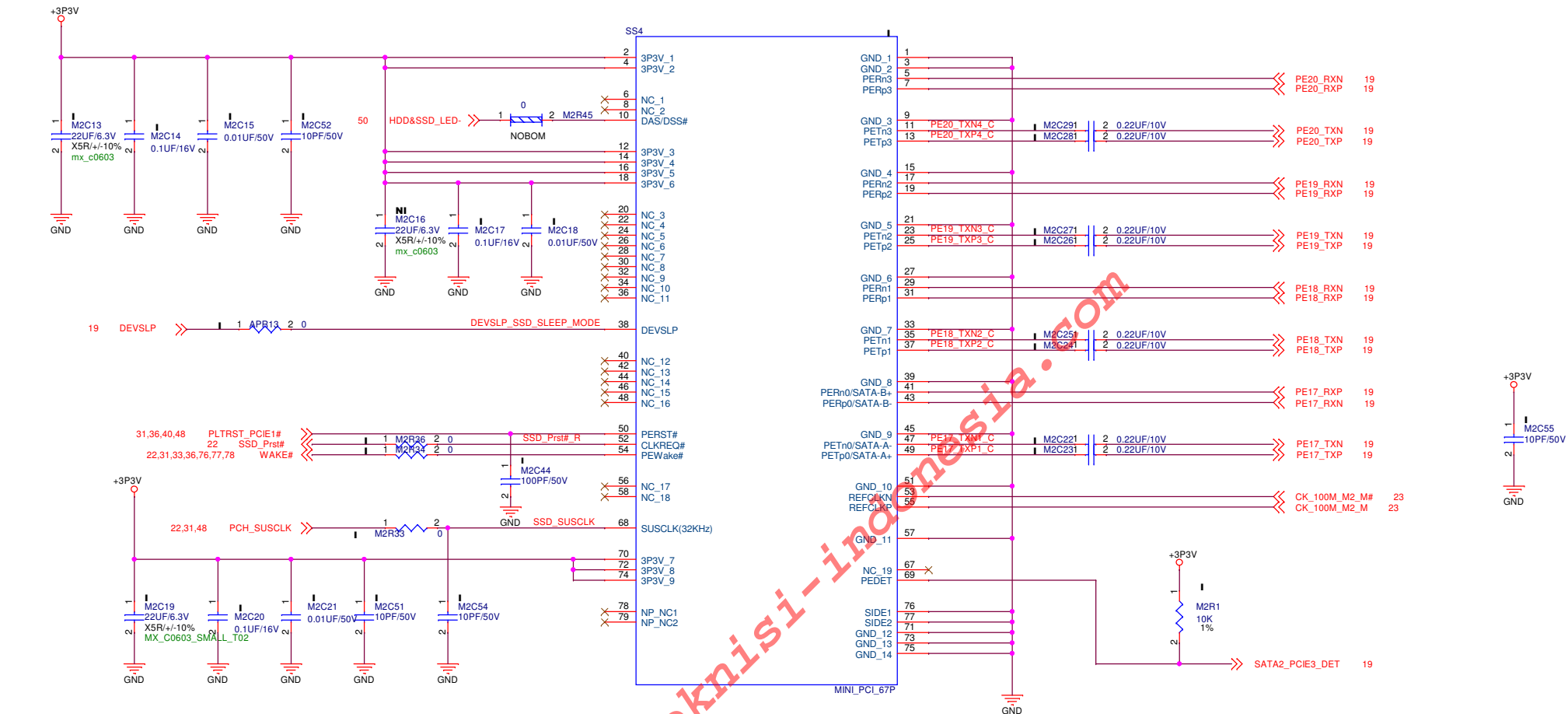
Battery Socket





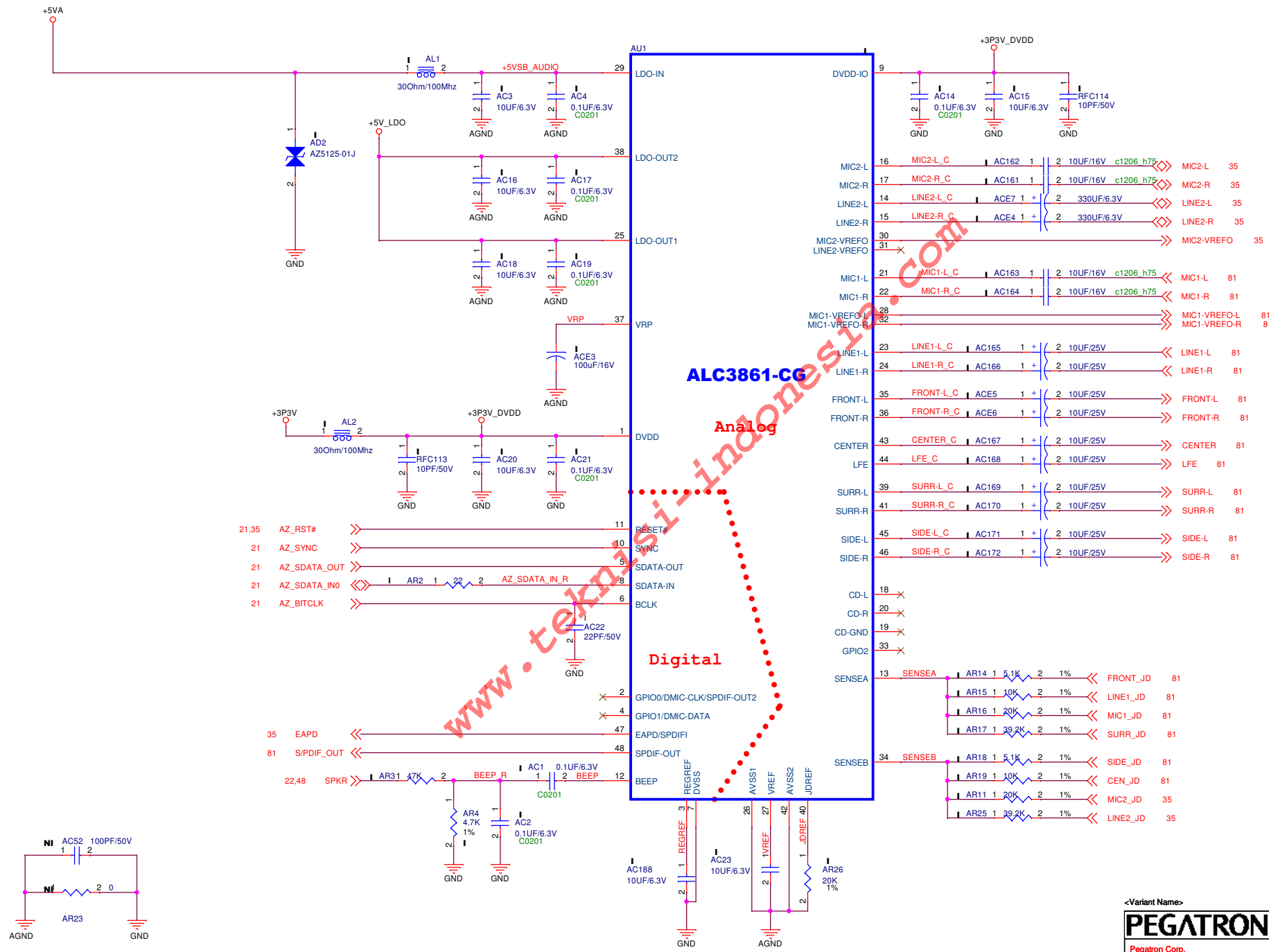


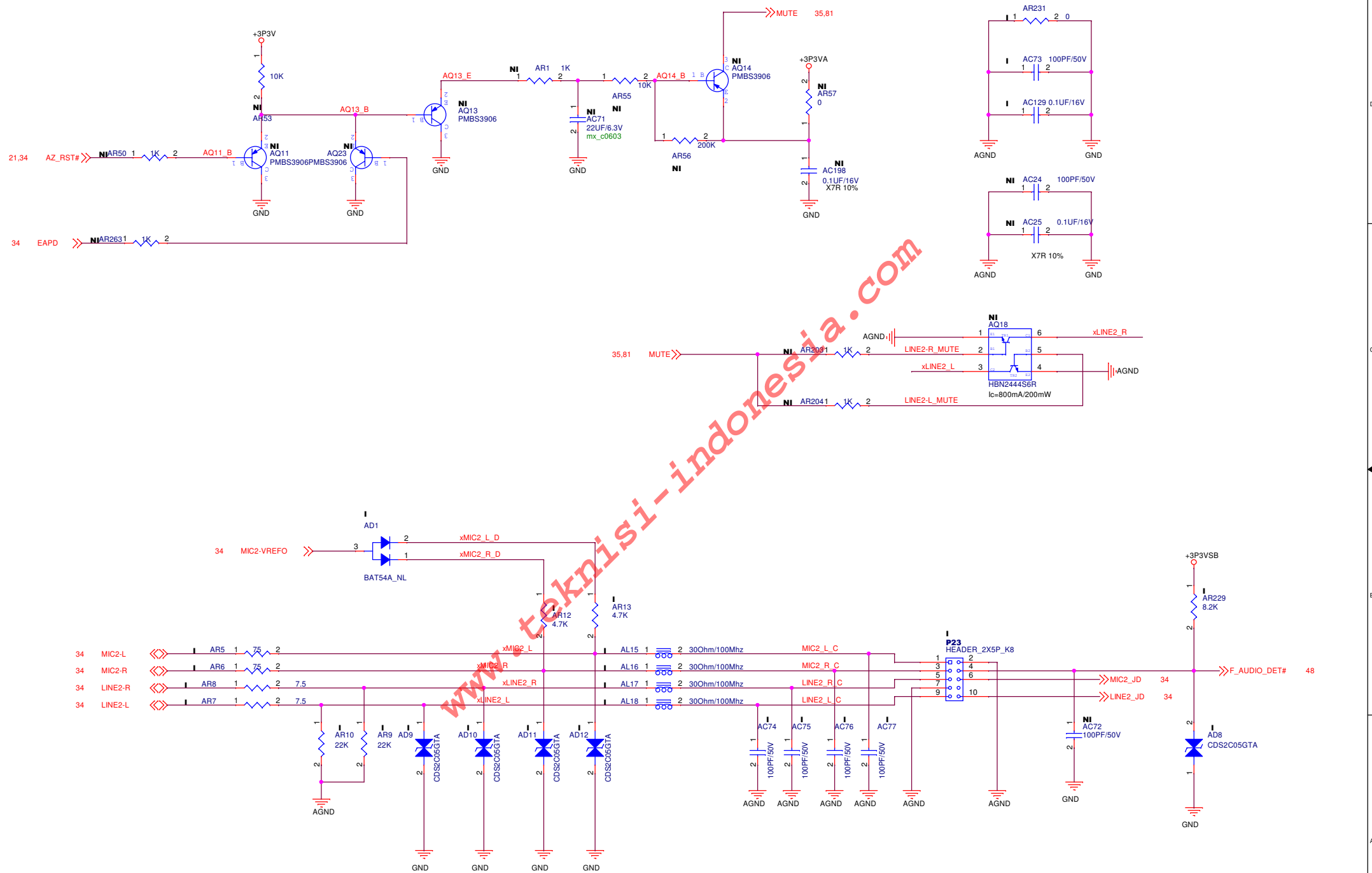


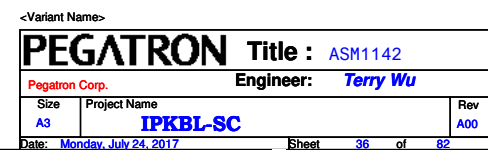


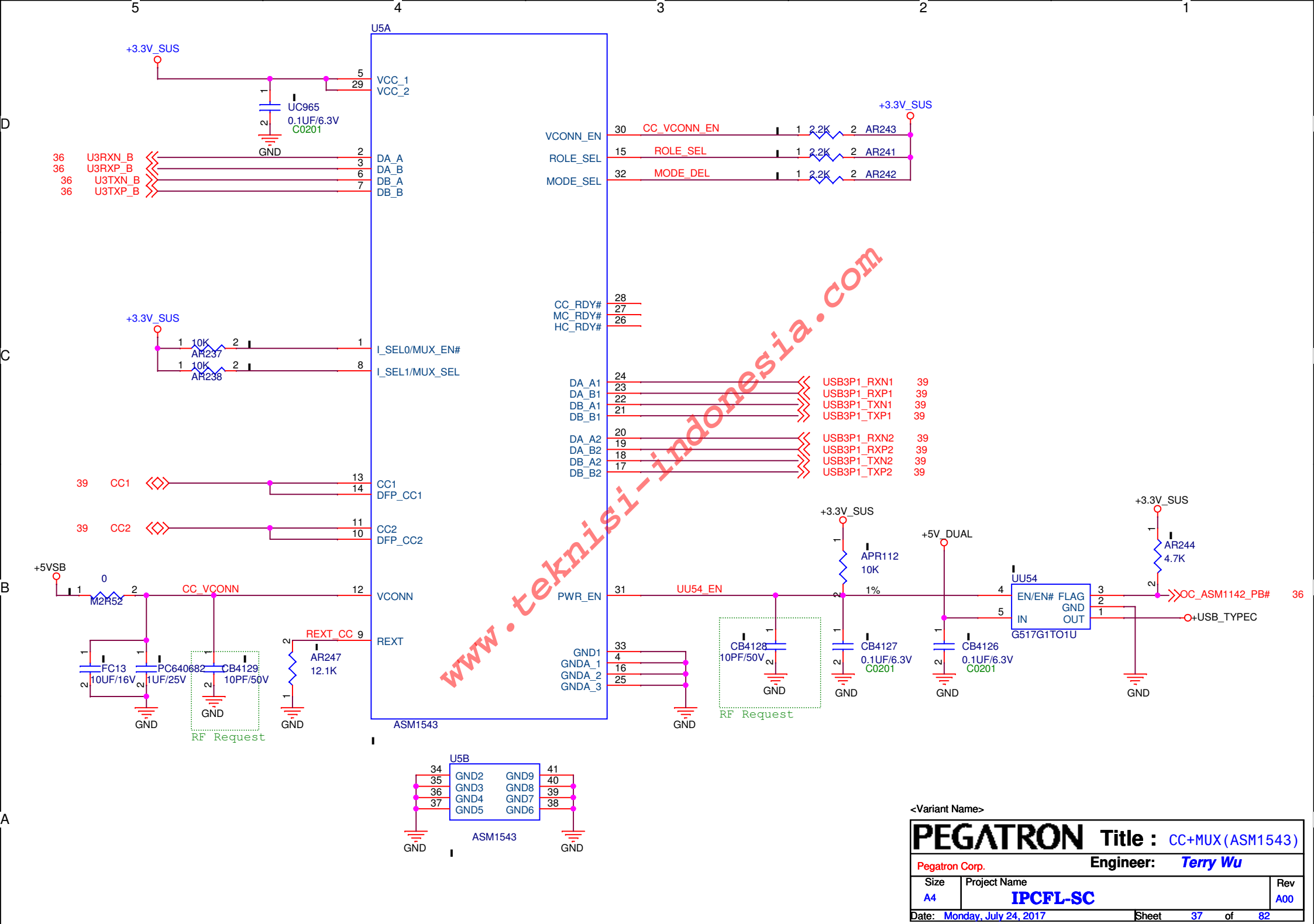








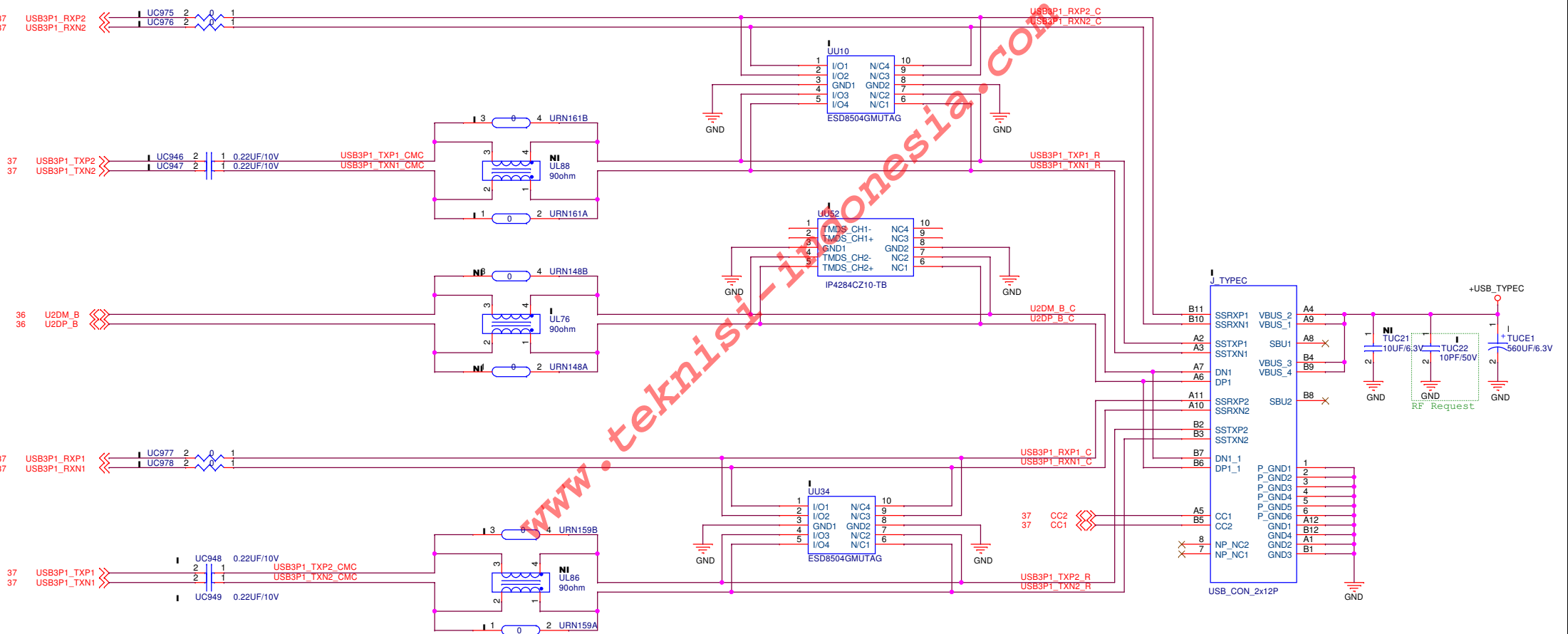


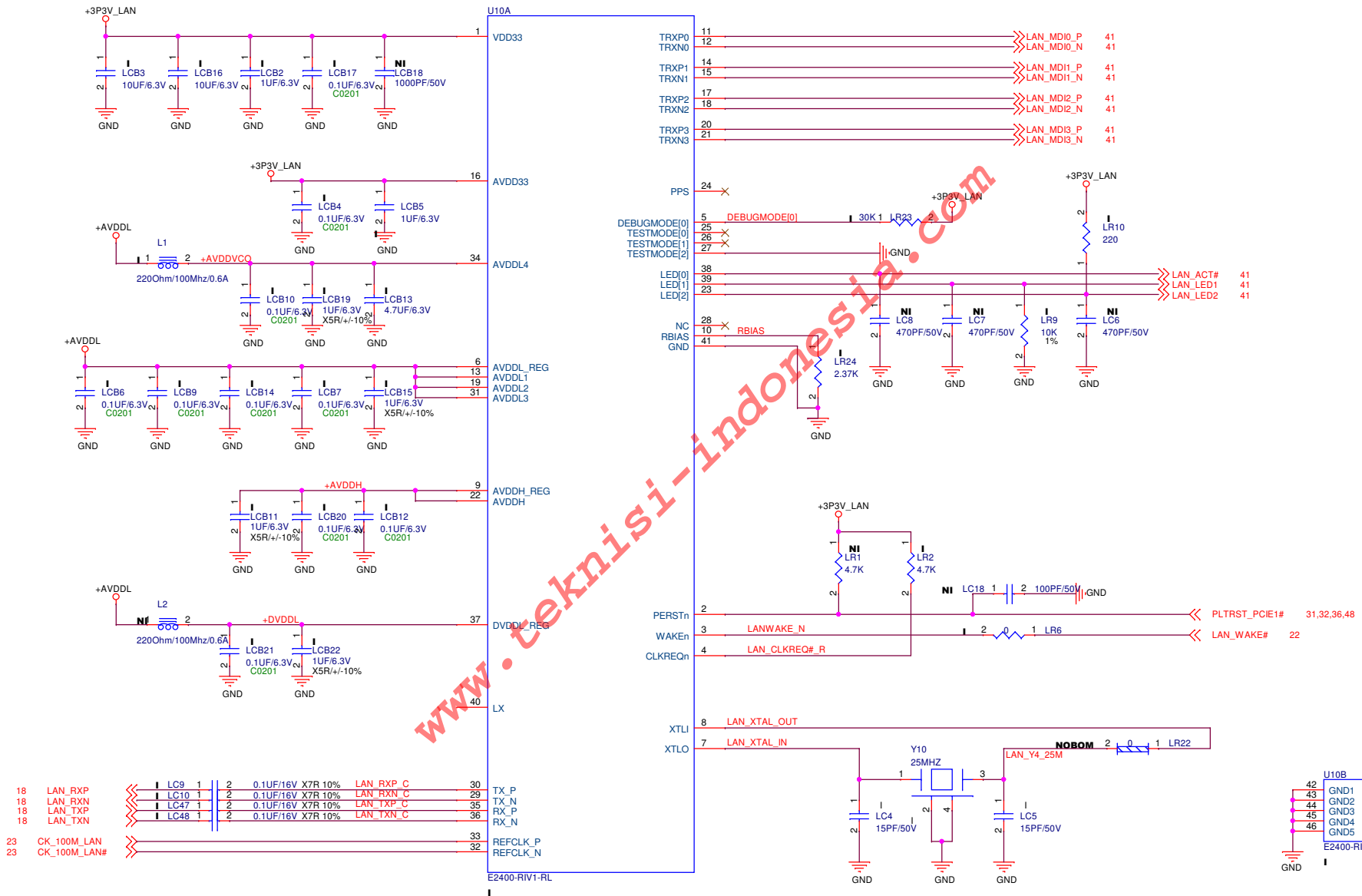


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# USB3.1(Type C) Pin define

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND





&lt;Variant Name&gt;

**PEGATRON** Title : LAN\_E2500

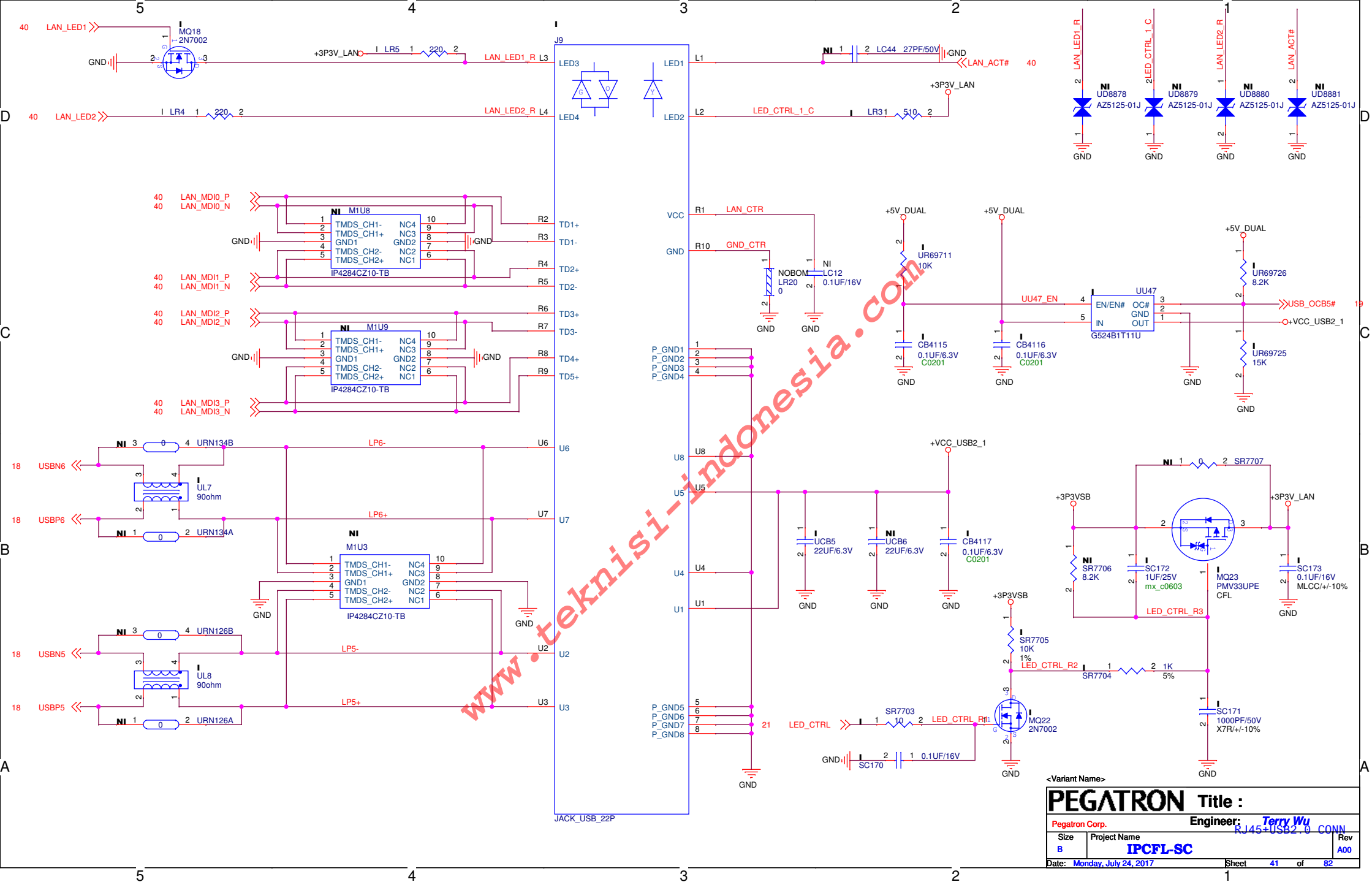
Pegatron Corp. Engineer: Terry Wu

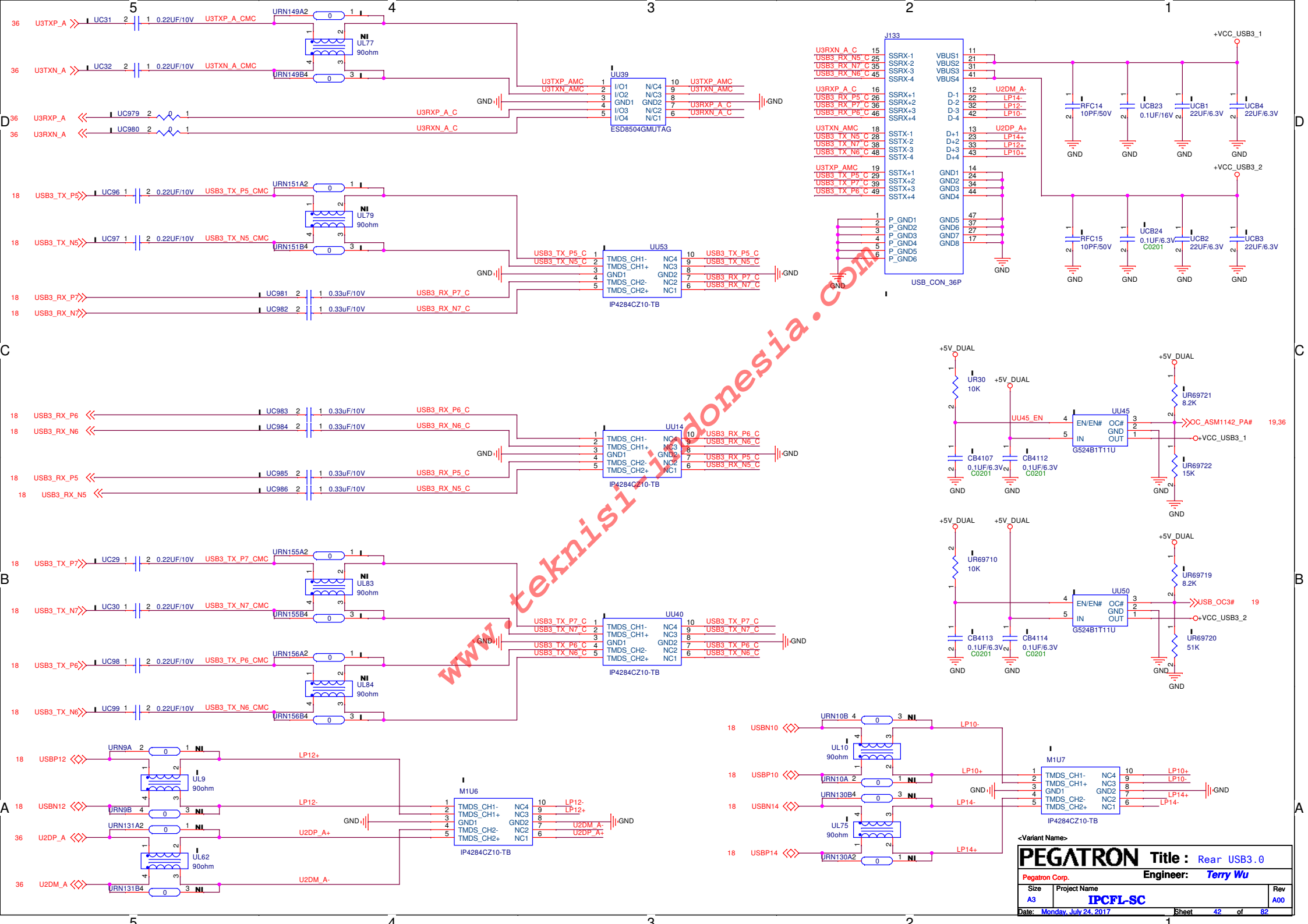
Size	Project Name	Rev
A3	IPCFL-SC	A00

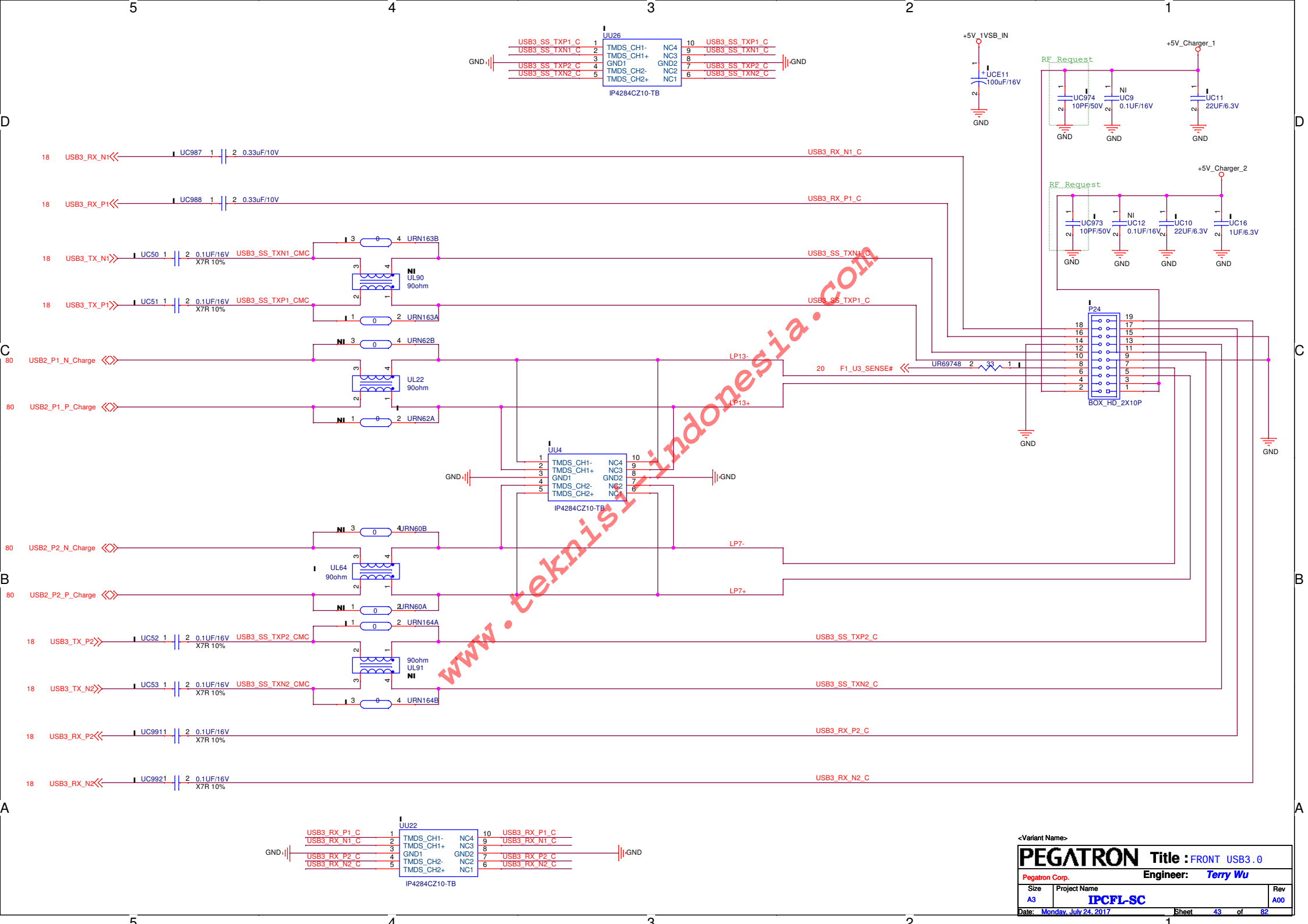
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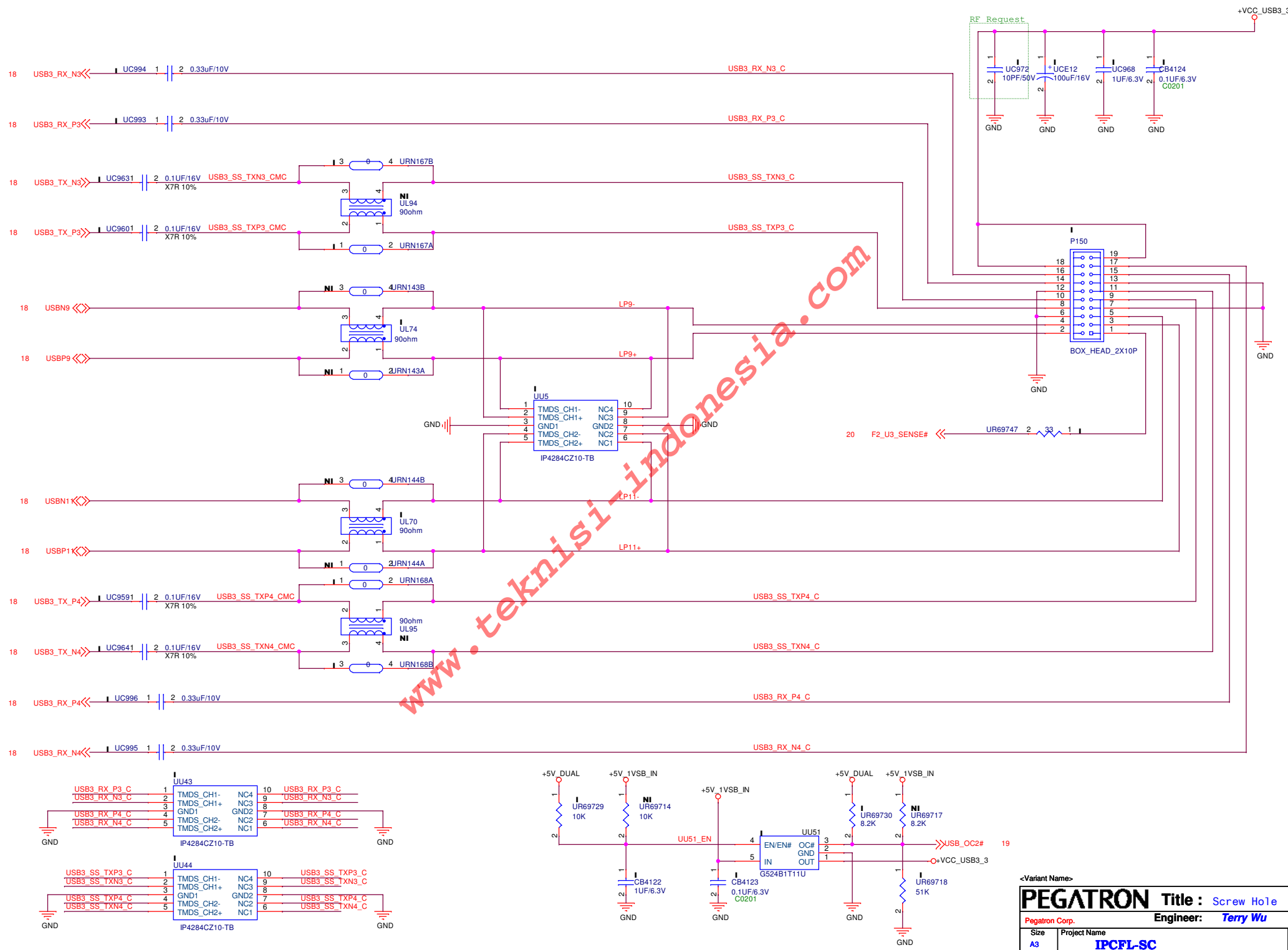
Sheet 40 of 82

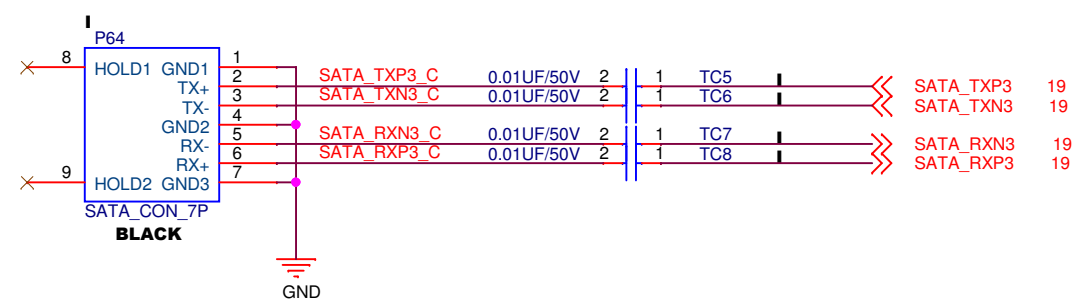
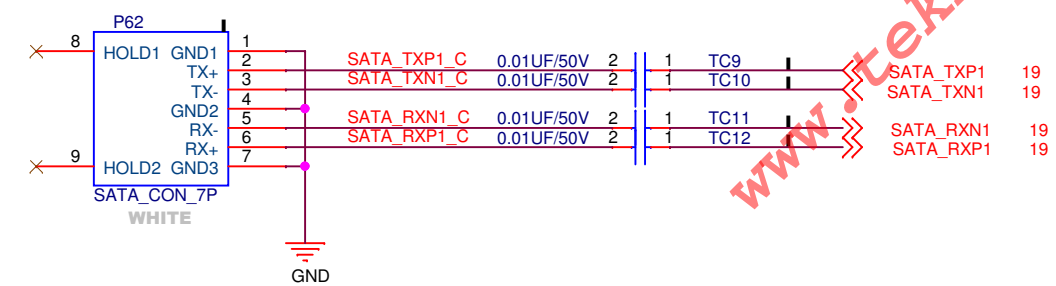
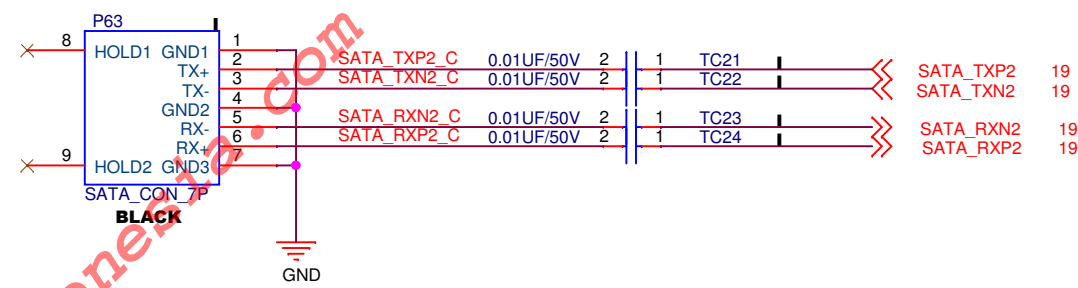
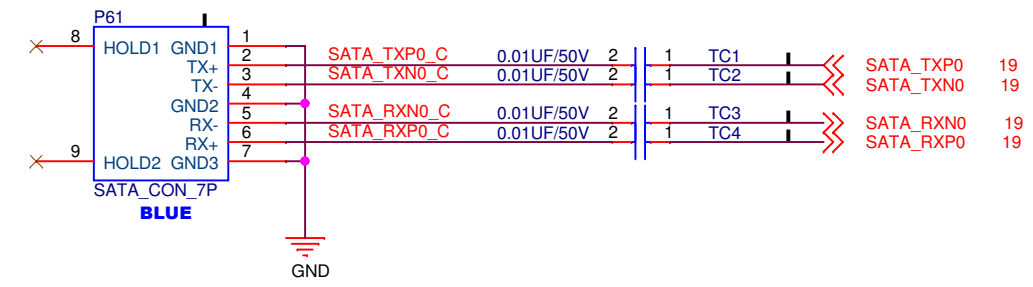


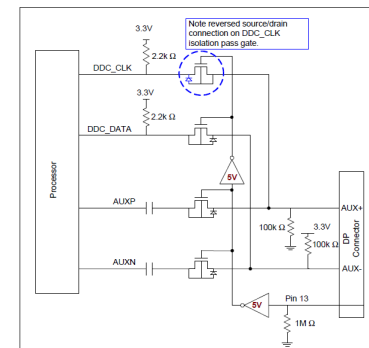
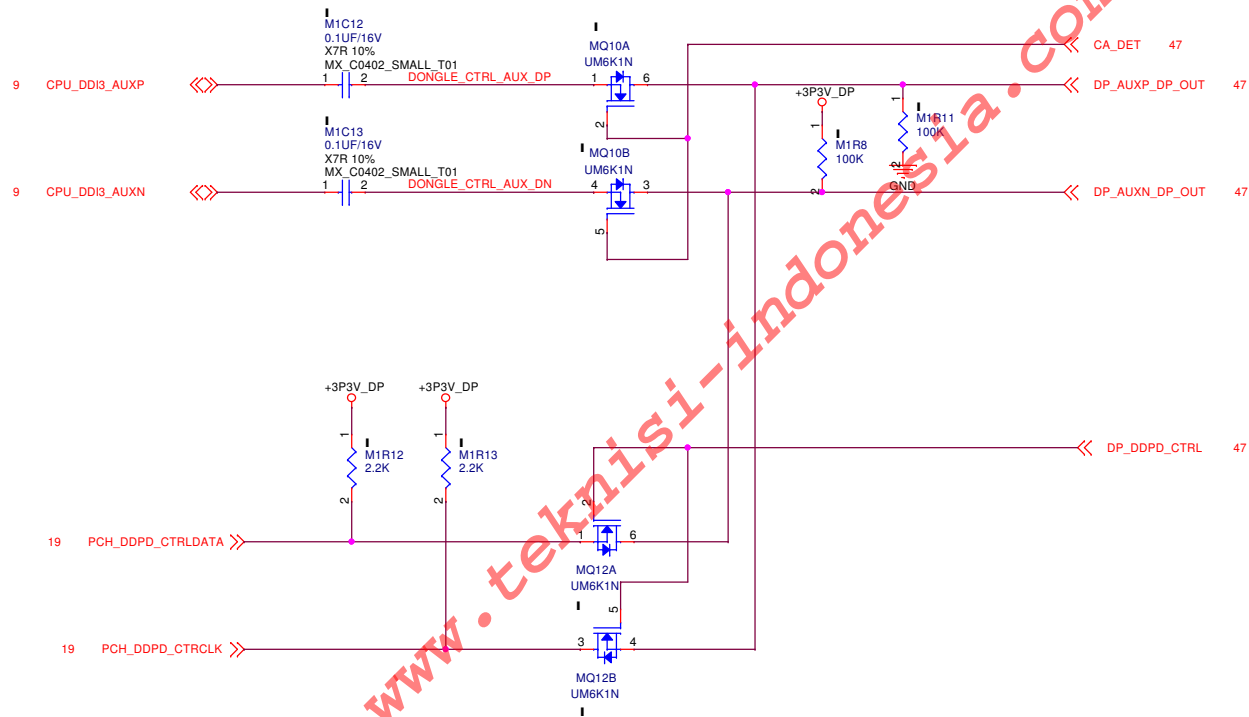






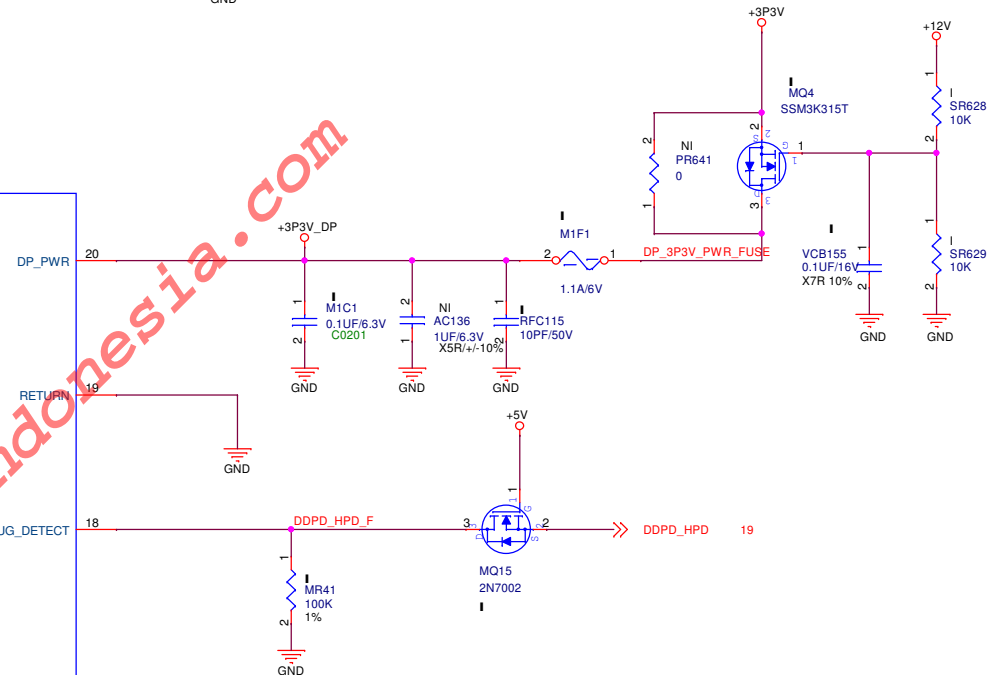


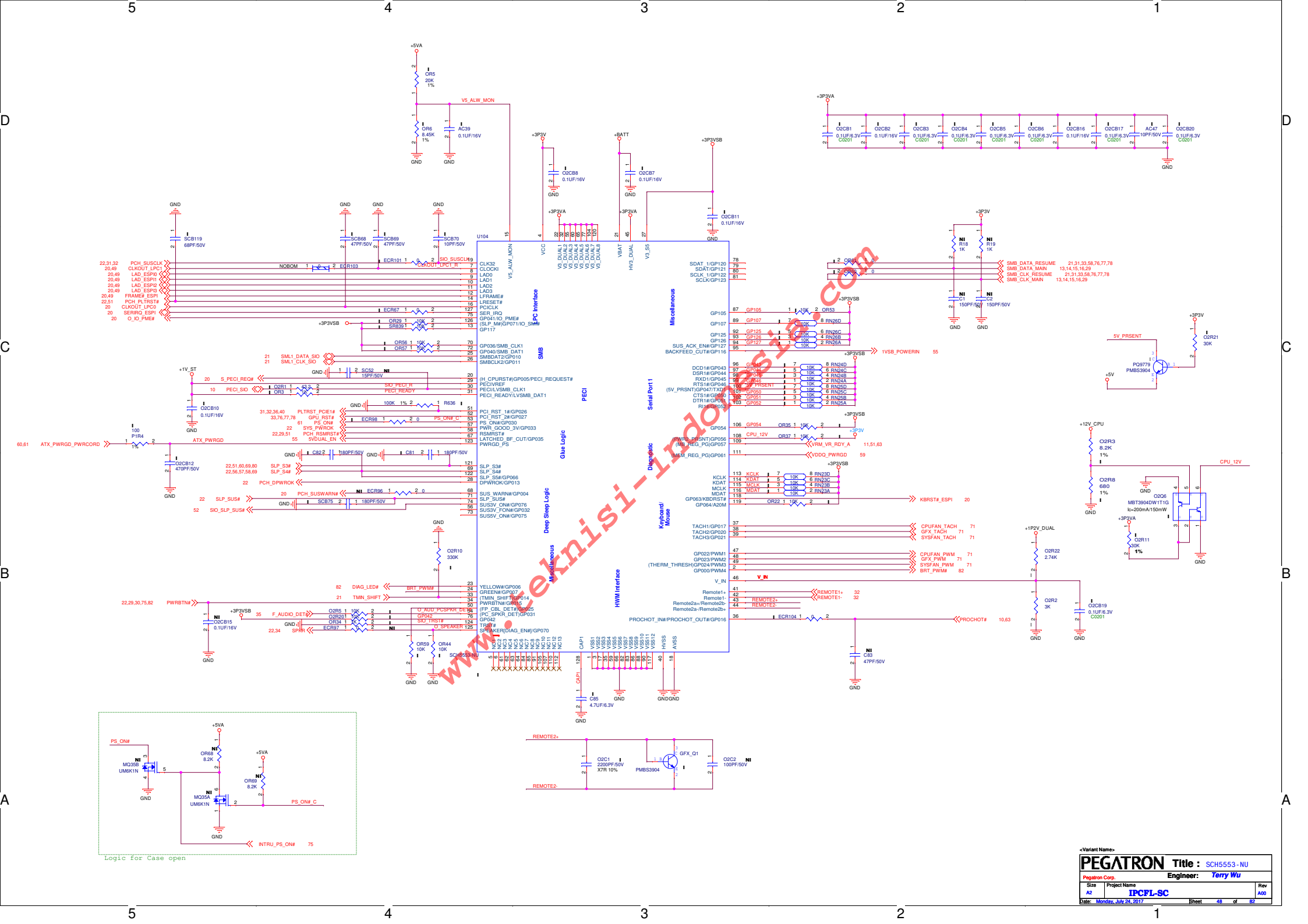




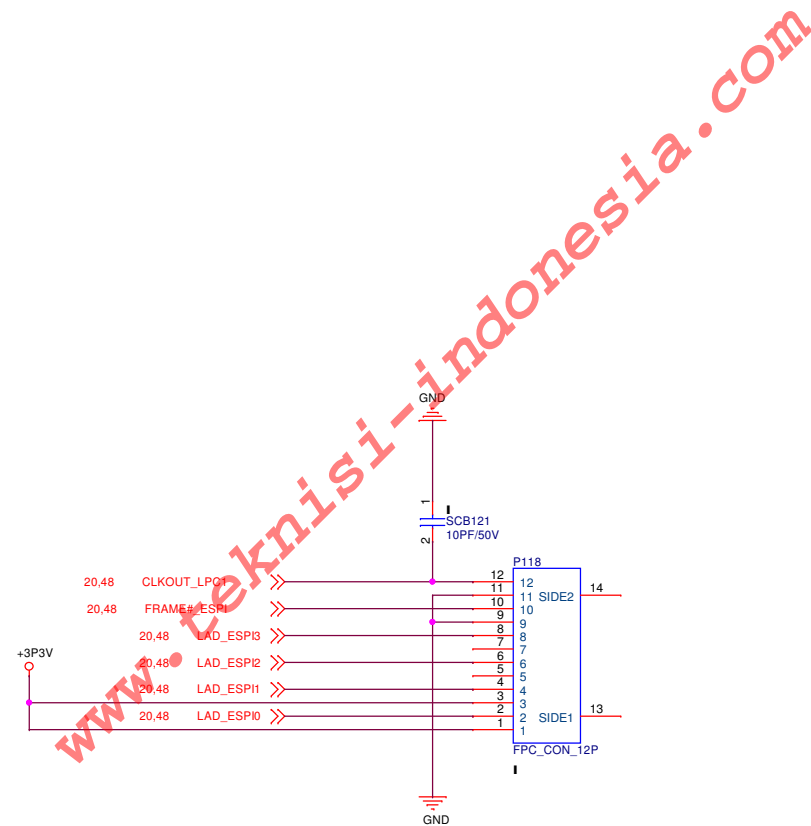
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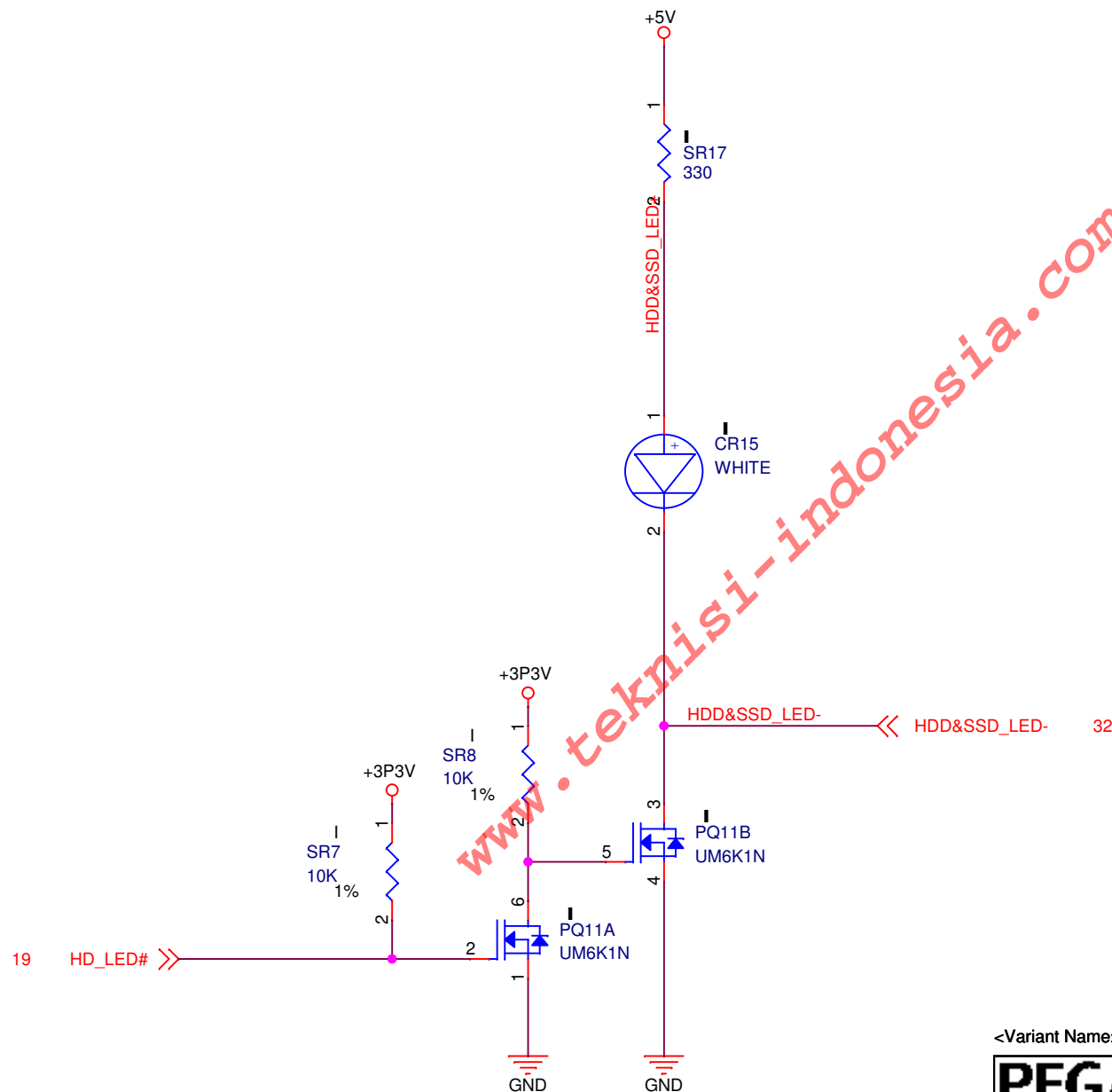
PEGATRON		Title : DP DONGLE CTRL	
Pegatron Corp.		Engineer: Terry Wu	
Size A3	Project Name IPCFL-SC	Rev A00	
Date: Monday, July 24, 2017		Sheet 46 of 82	







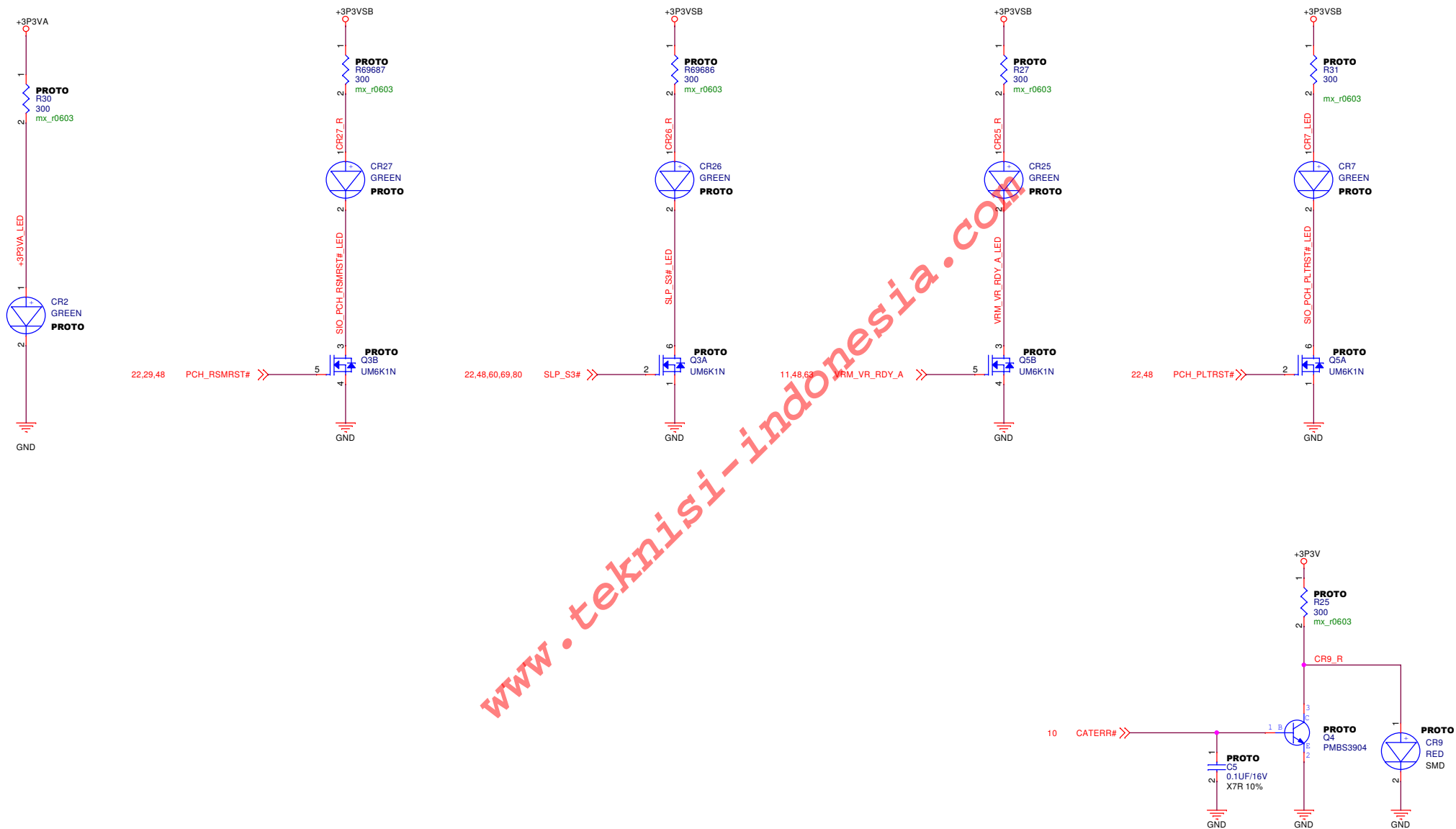


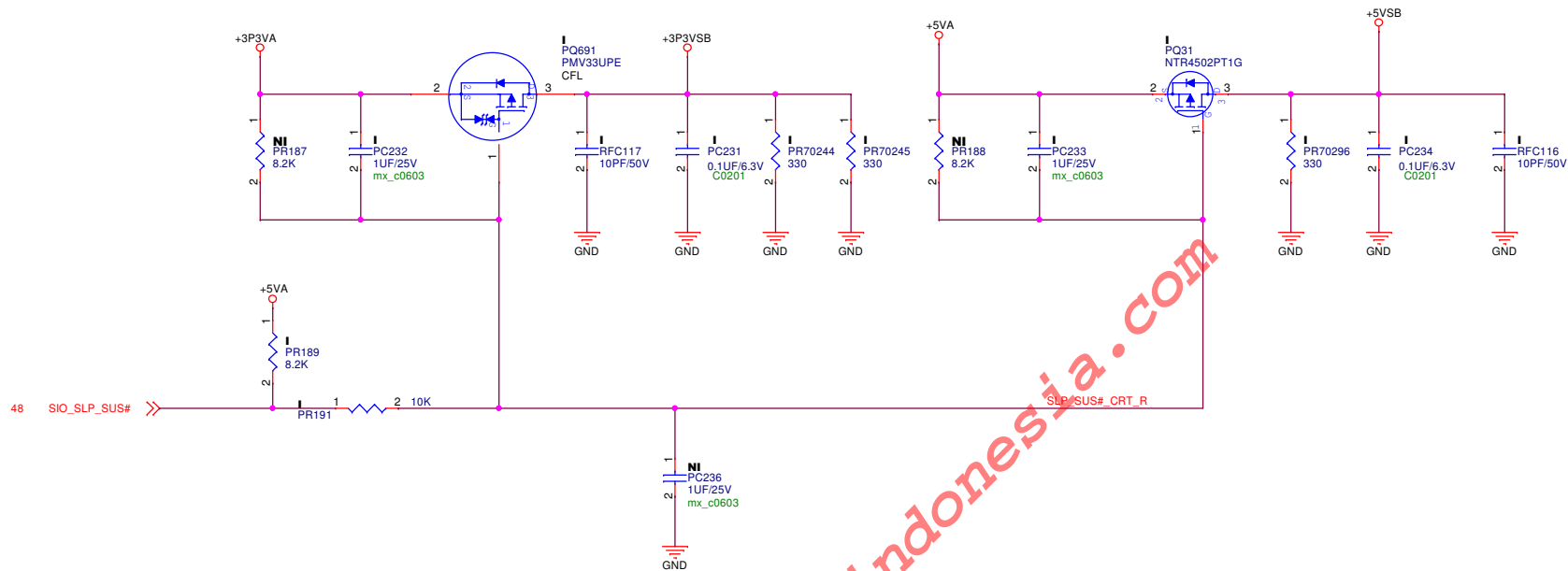


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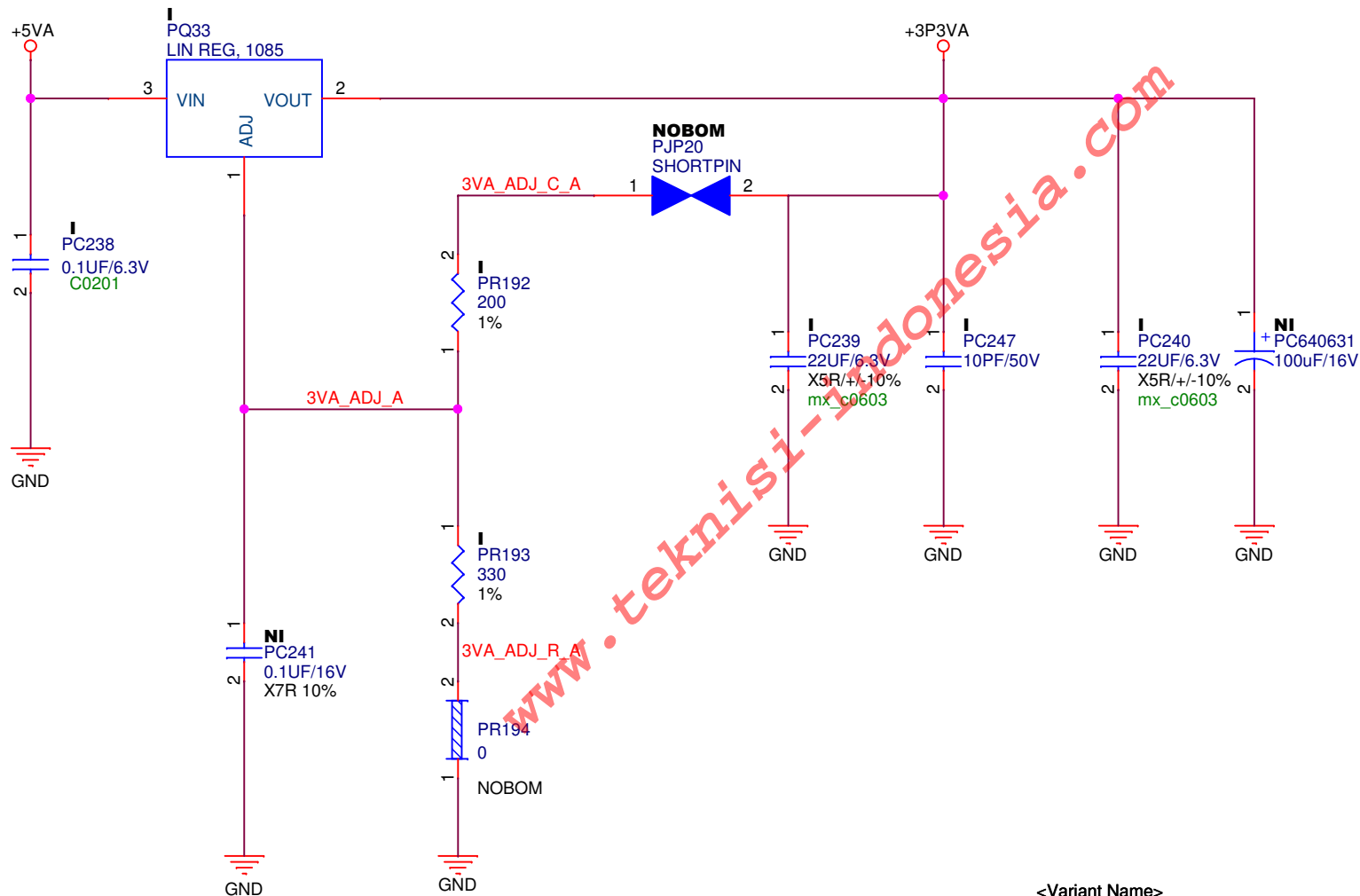
<b>PEGATRON</b>		Title :	
Pegatron Corp.		Engineer: <b>Terry Wu</b>	
Size <b>A</b>	Project Name <b>IPCFL-SC</b>		Rev <b>A00</b>
Date: <b>Monday, July 24, 2017</b>	Sheet <b>50</b> of <b>82</b>		

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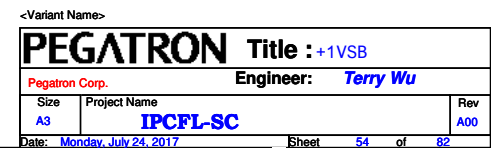


<Variant Name>

<b>PEGATRON</b>		Title :	+3P3VA
Pegatron Corp.		Engineer:	Terry Wu
Size A	Project Name <b>IPCFL-SC</b>		Rev A00
Date: Monday, July 24, 2017	Sheet 53 of 82		

$R_{RF}$ (k $\Omega$ )	Switching Frequency (kHz)
470k $\Omega$	290
200k $\Omega$	340
100k $\Omega$	380
39k $\Omega$	430

Note : For DEM, connect  $R_{RF}$  to GND; for CCM, connect  $R_{RF}$  to PGOOD.





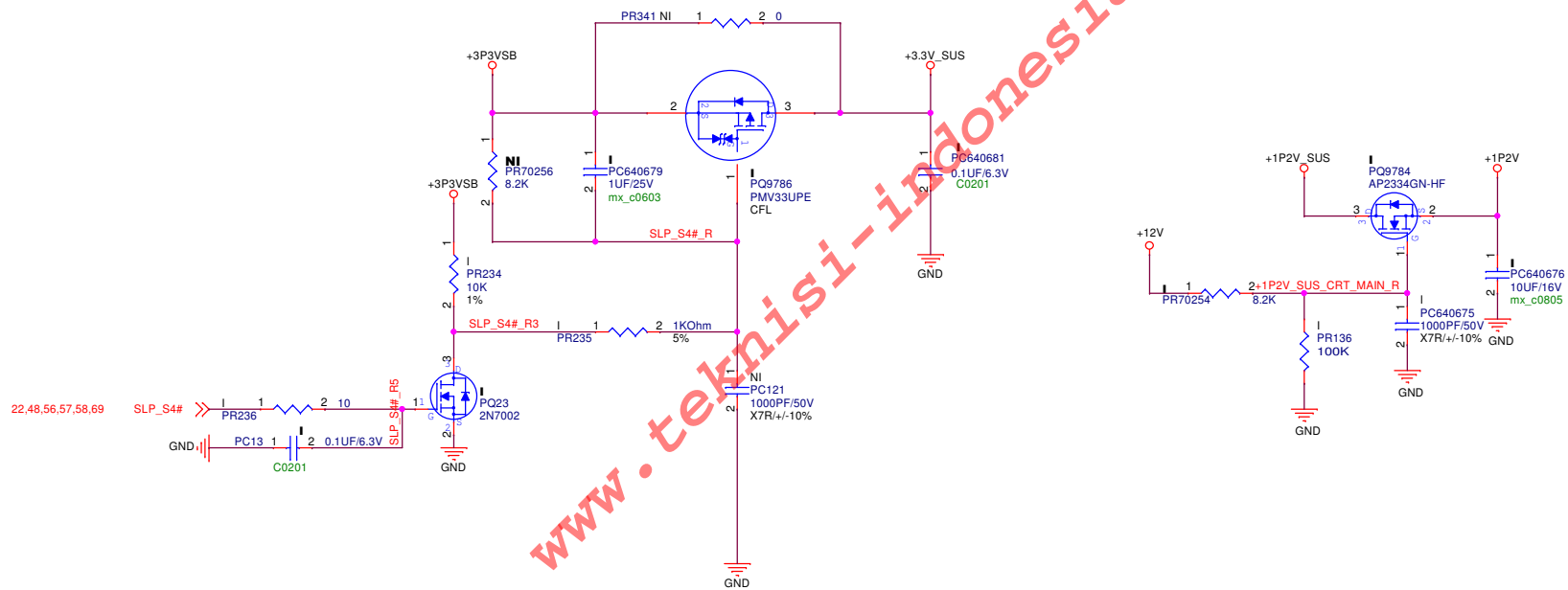
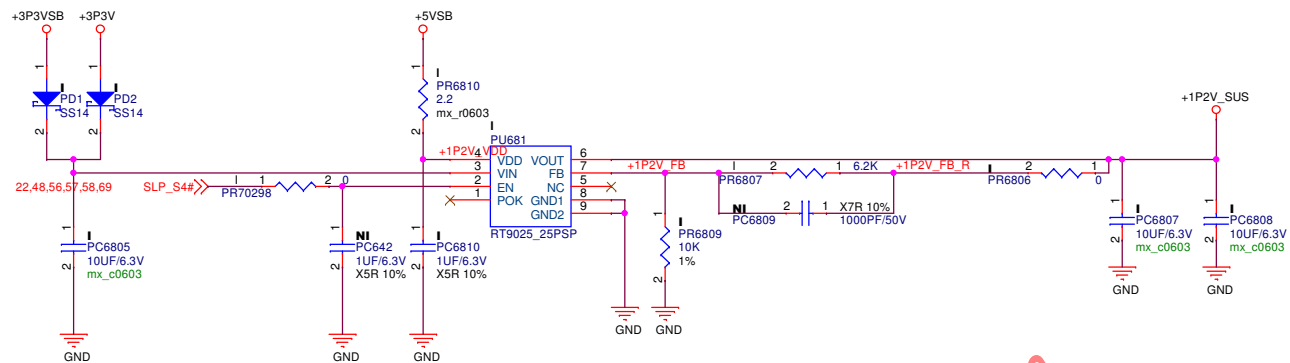
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4

3

2

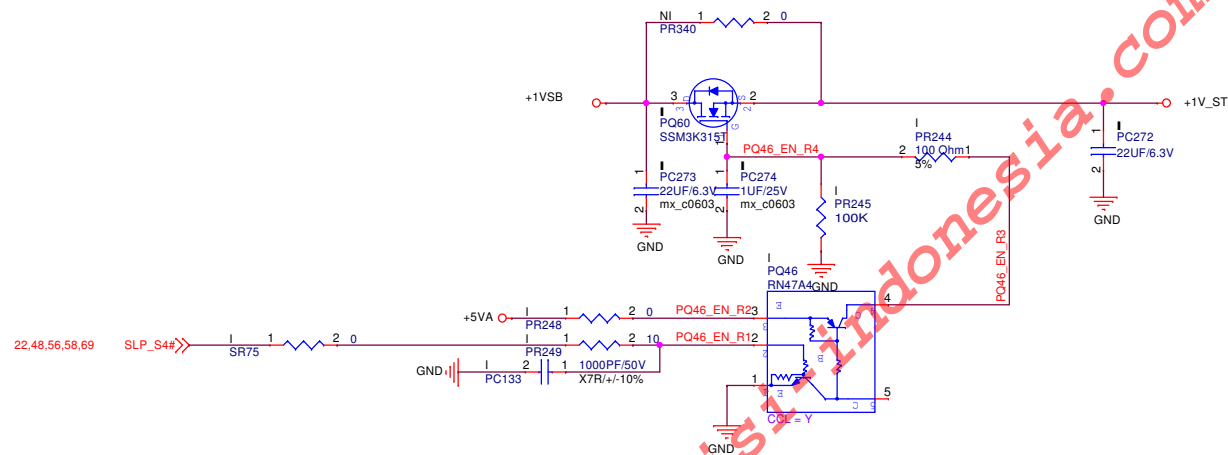
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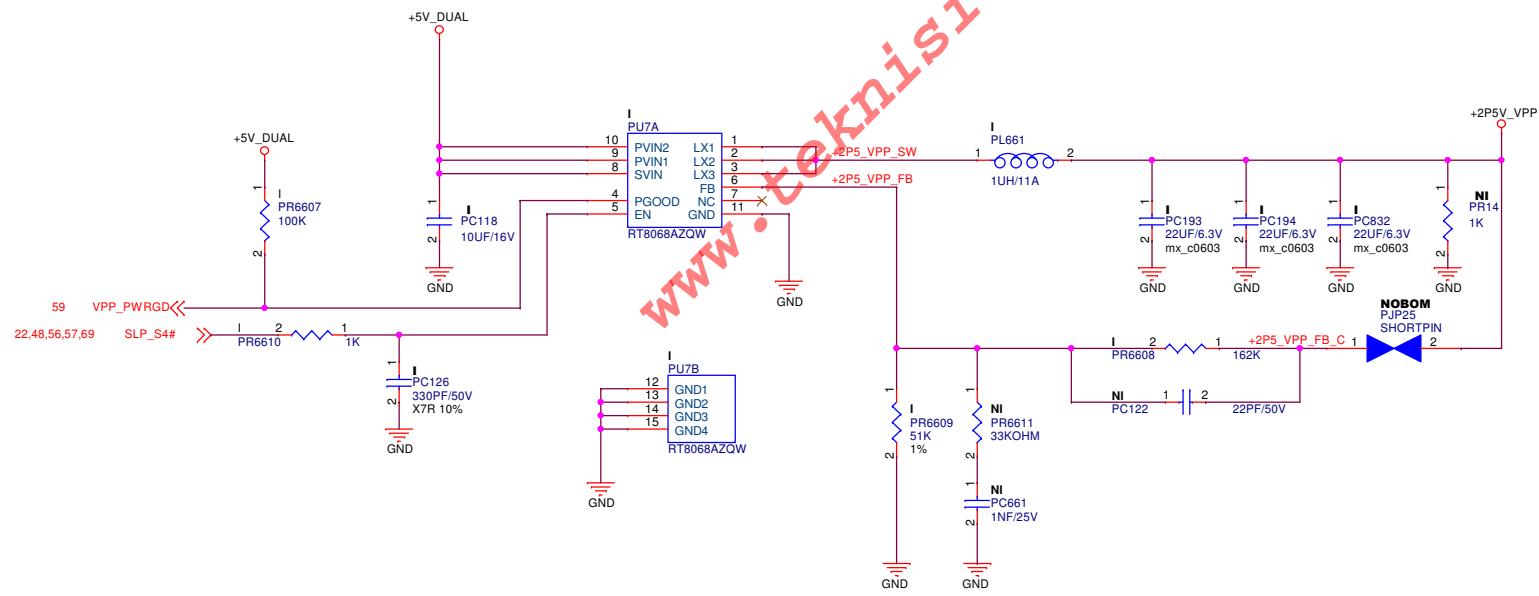
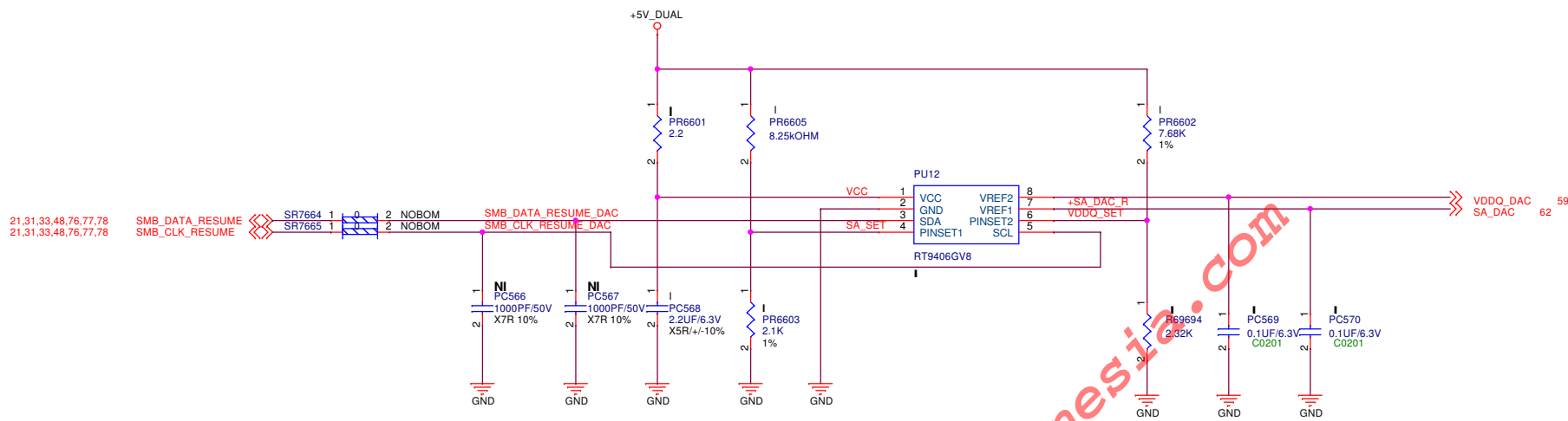
PEGATRON		Title : +1P2V	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name	Rev	
A3	IPCFL-SC	A00	
Date: Monday, July 24, 2017		Sheet 56 of 82	





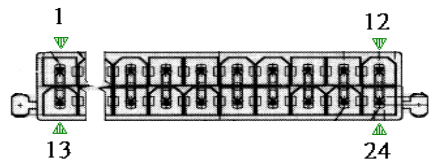
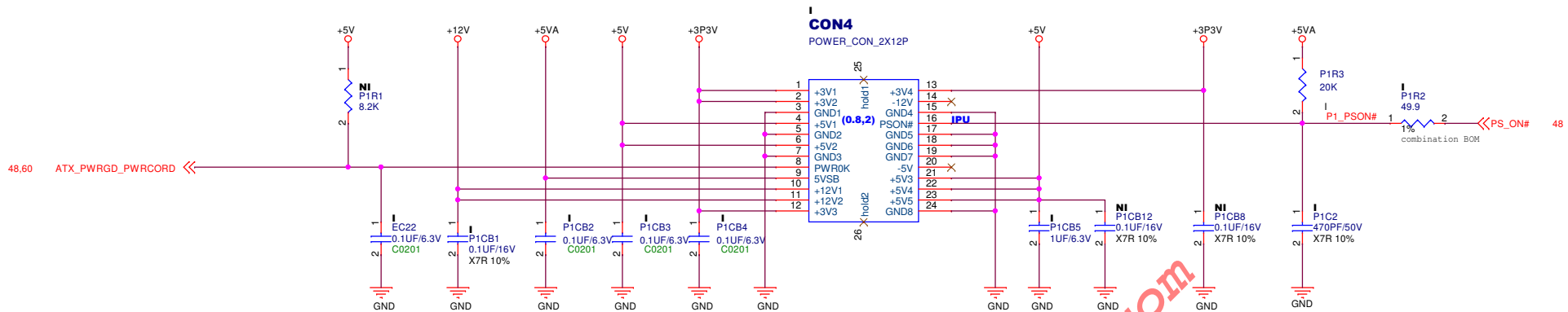
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PEGATRON		Title : +1P2V	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name		Rev
A3	IPCFL-SC		A00
Date: Monday, July 24, 2017		Sheet 57 of 82	

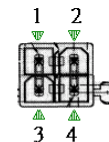




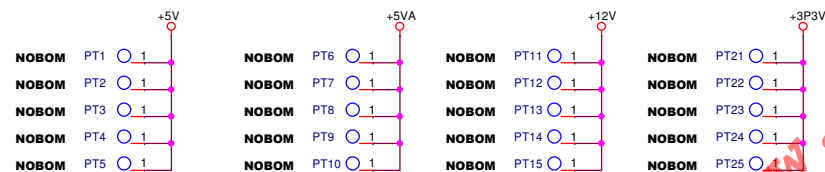
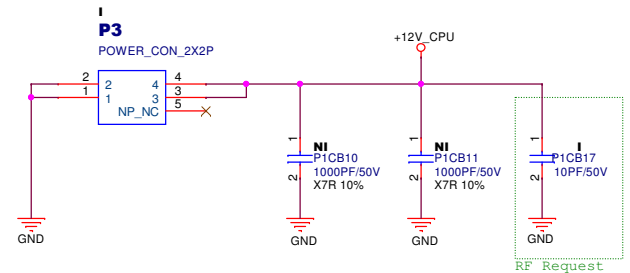




TOP SIDE VIEW

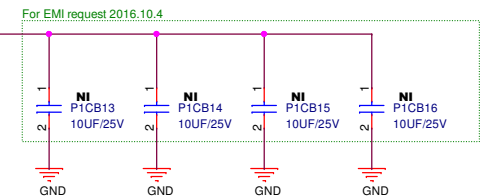


TOP SIDE VIEW



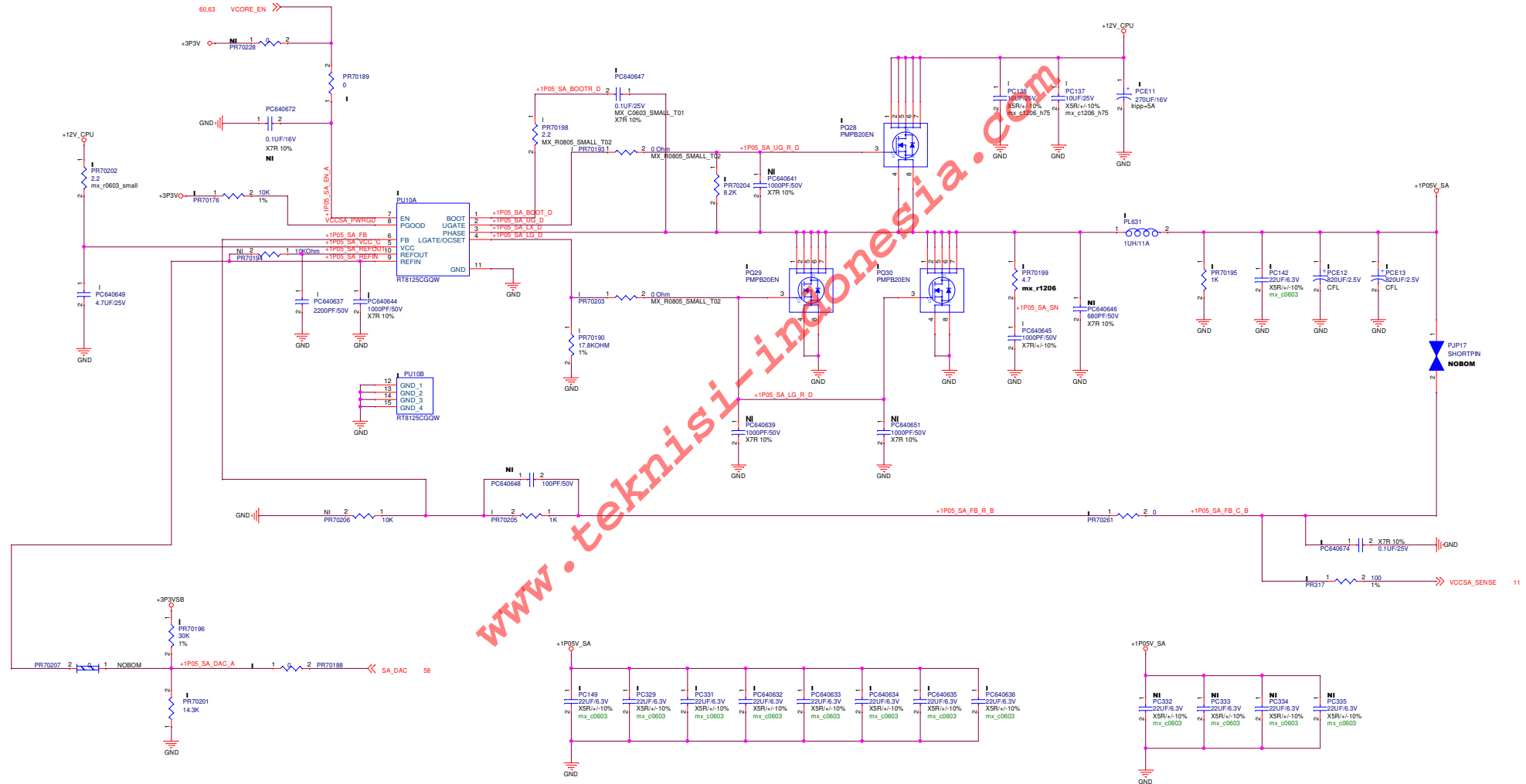
Nodes related to different power planes

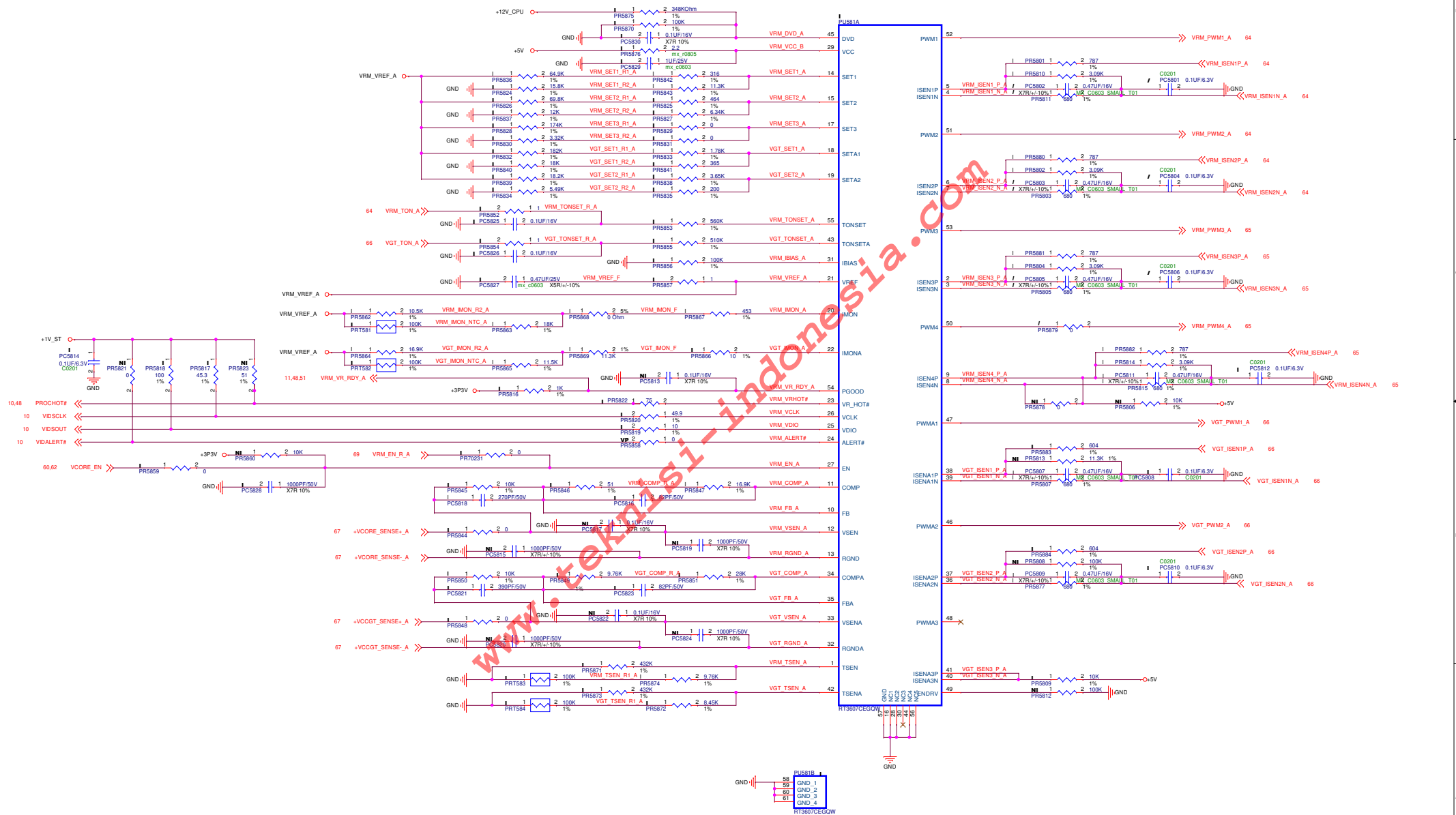
Node	Goal Q'ty
+5V	5
+5VA	5
+12V	5
-12V	5
+3V	5
+Vcore	10
+GND	15
+12V_CPU	10

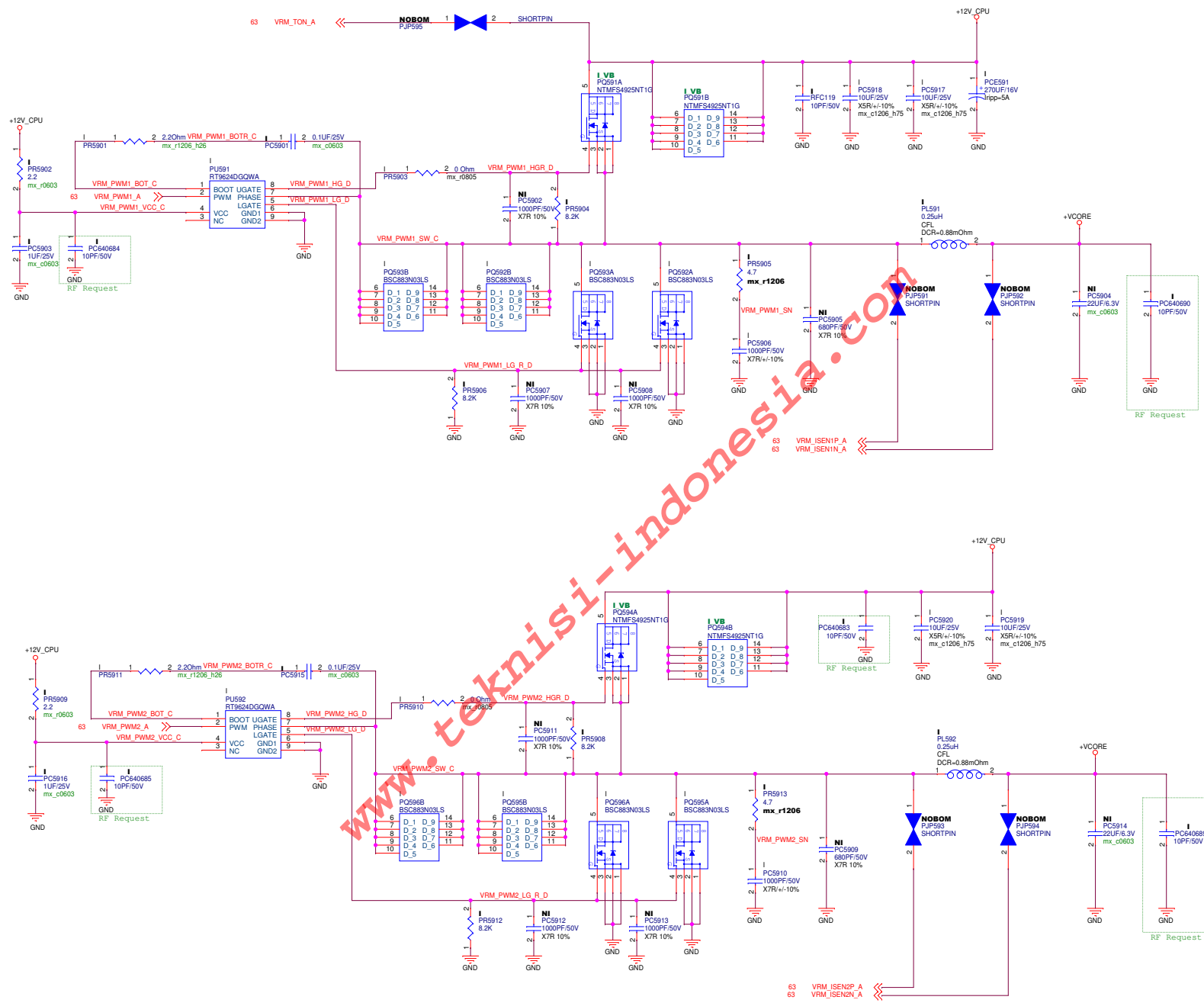


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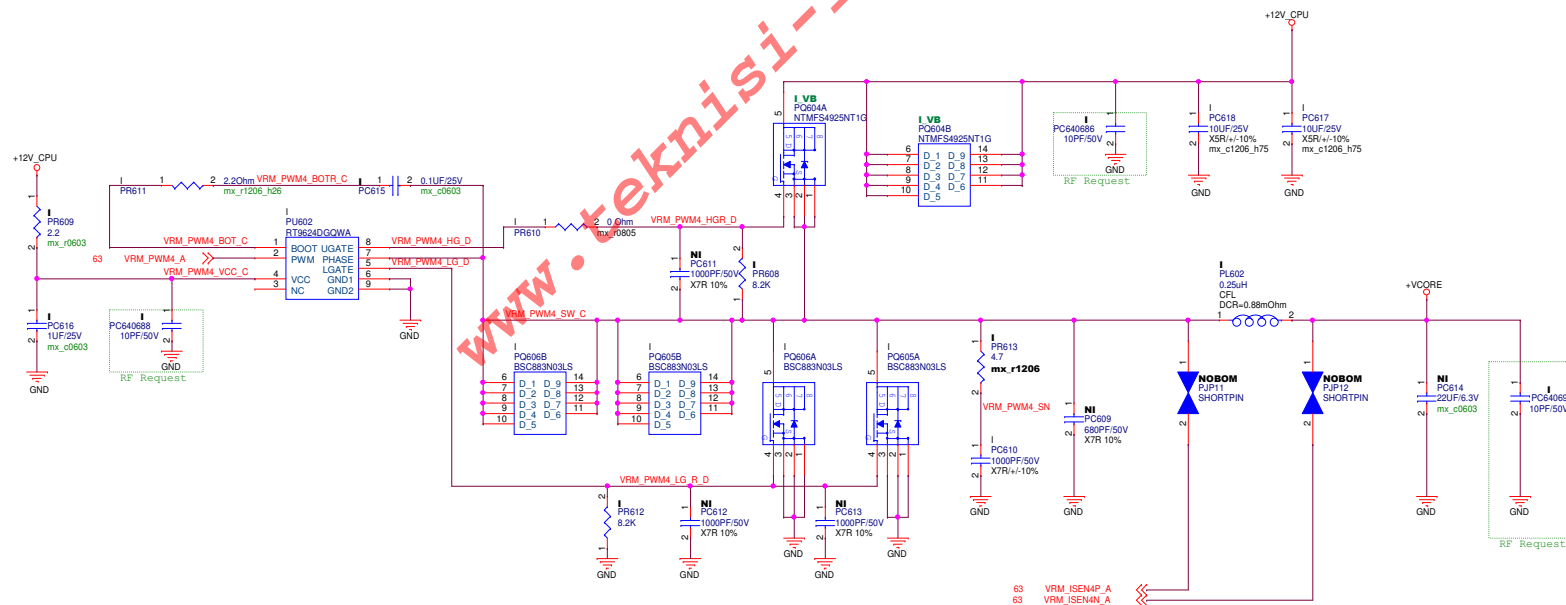
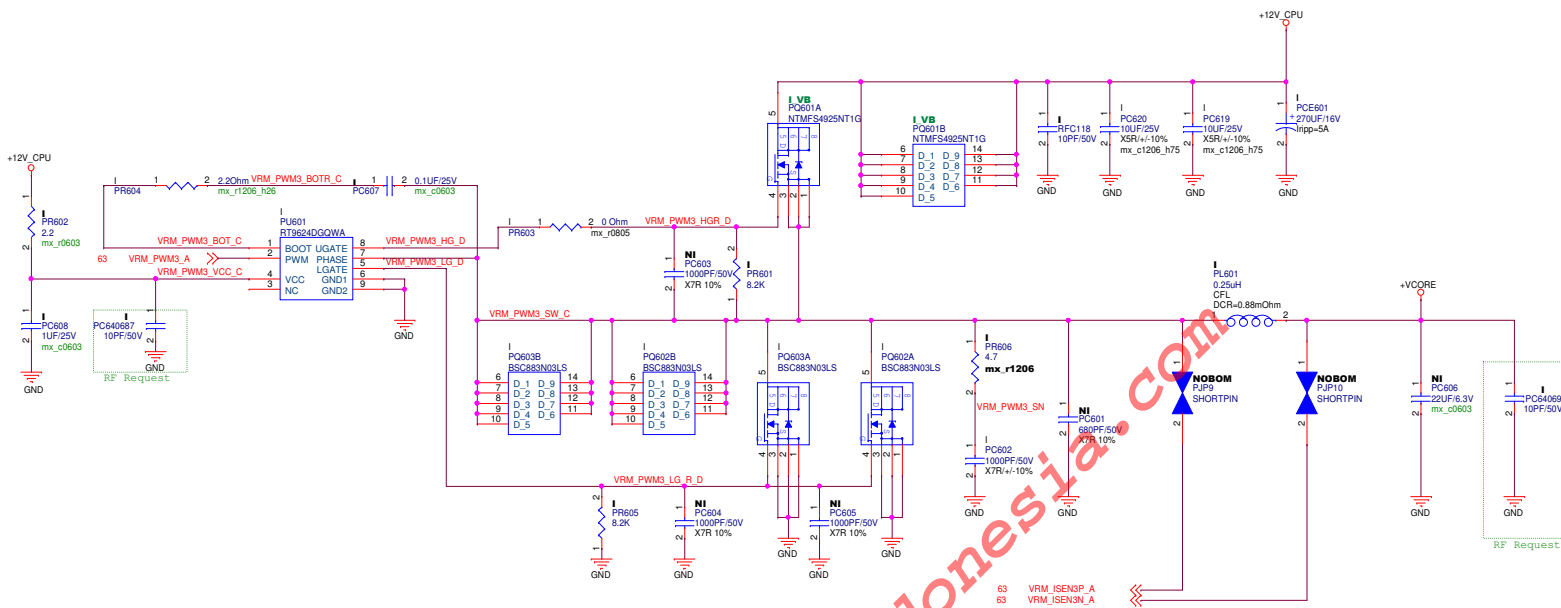
<b>PEGATRON</b>		Title : ATX POWER	
Pegatron Corp.		Engineer: Terry Wu	
Size A3	Project Name IPCFL-SC	Rev A00	
Date: Monday, July 24, 2017		Sheet	61 of 82



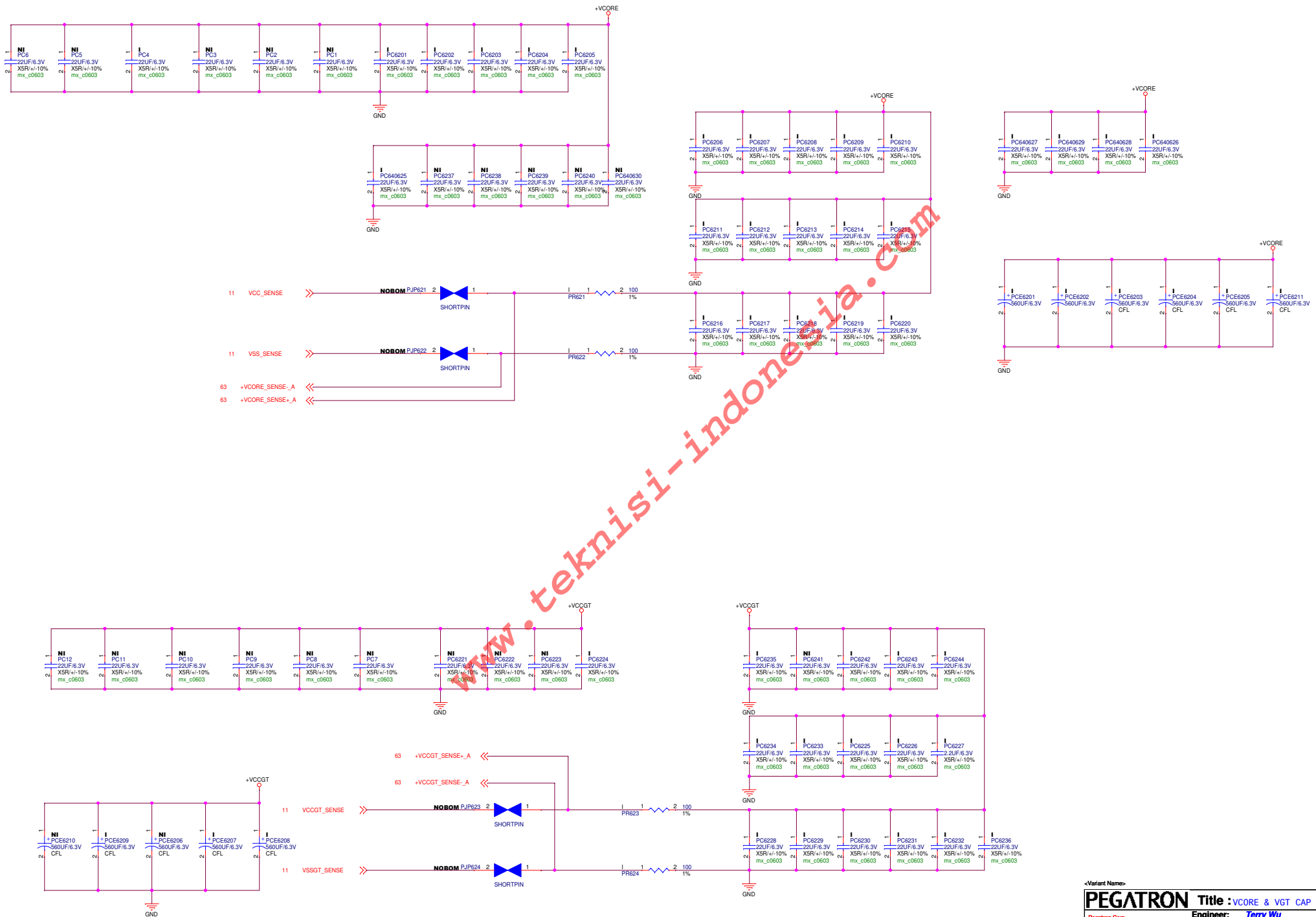




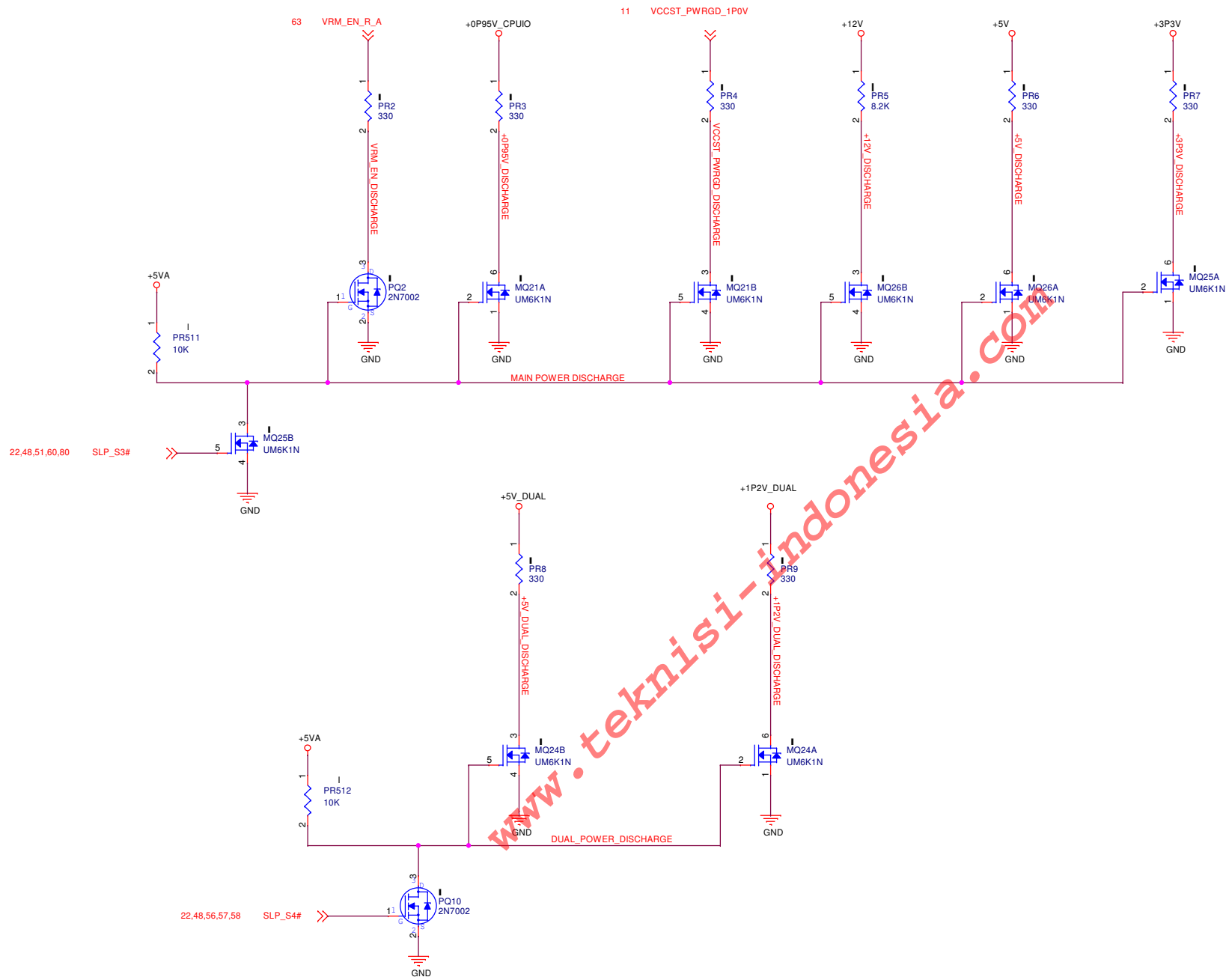




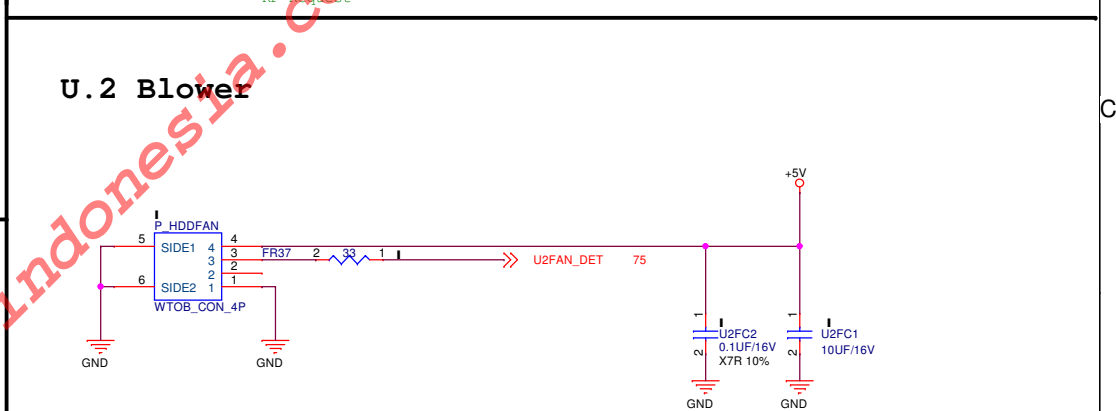
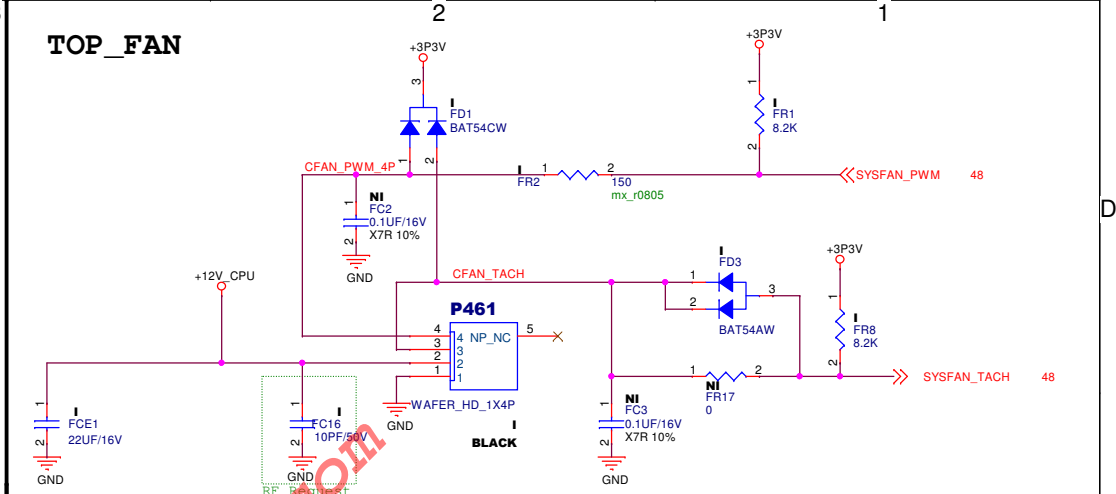
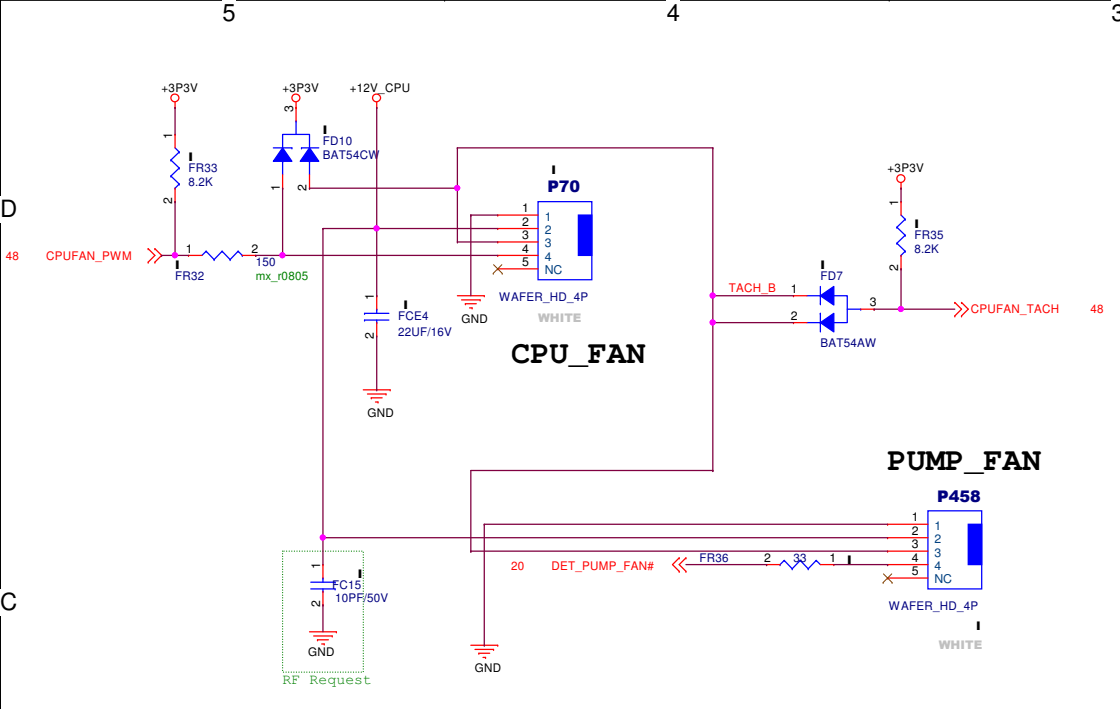









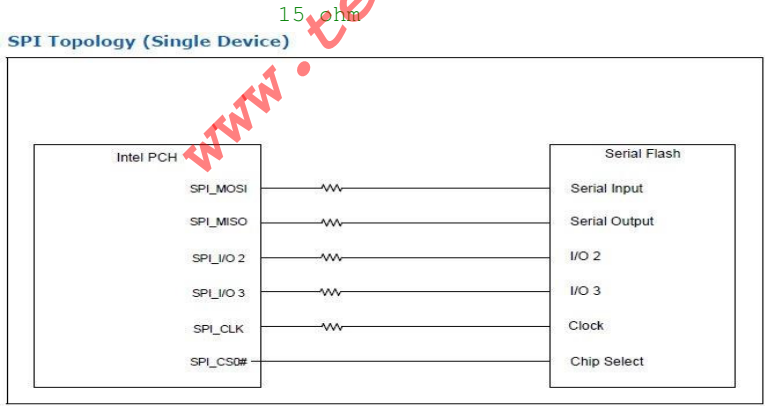
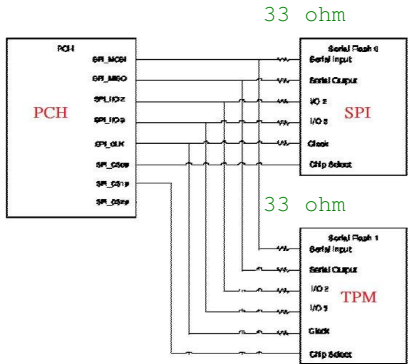
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TOLERANCES				CABLE	
HOLES : $\pm 0.15$				HOUSING: JWT A1251H02-4PA-HF OR EQUIVALENT.	
ANGLES : $\pm 2.0^\circ$				TERMINAL: JWT A1251T0P-2 OR EQUIVALENT.	
$<1.0$ : $\pm 0.10$ $1.0 \sim 10$ : $\pm 0.20$ $10 \sim 50$ : $\pm 0.30$ $ABOVE 50$ : $\pm 0.40$				H/S TUBE: $\phi 2.0 \times T: 0.2$ , COLOR: BLACK 125°C 300V	
 THIRD ANGLE PROJECTION				CABLE WIRE UL13302 AWG#30	
SCALE ---				PIN 1: BLACK -----(-)	
UNIT mm				PIN 2: BLUE -----(PWM)	
				PIN 3: YELLOW -----(O/P)	
				PIN 4: RED -----(+)	

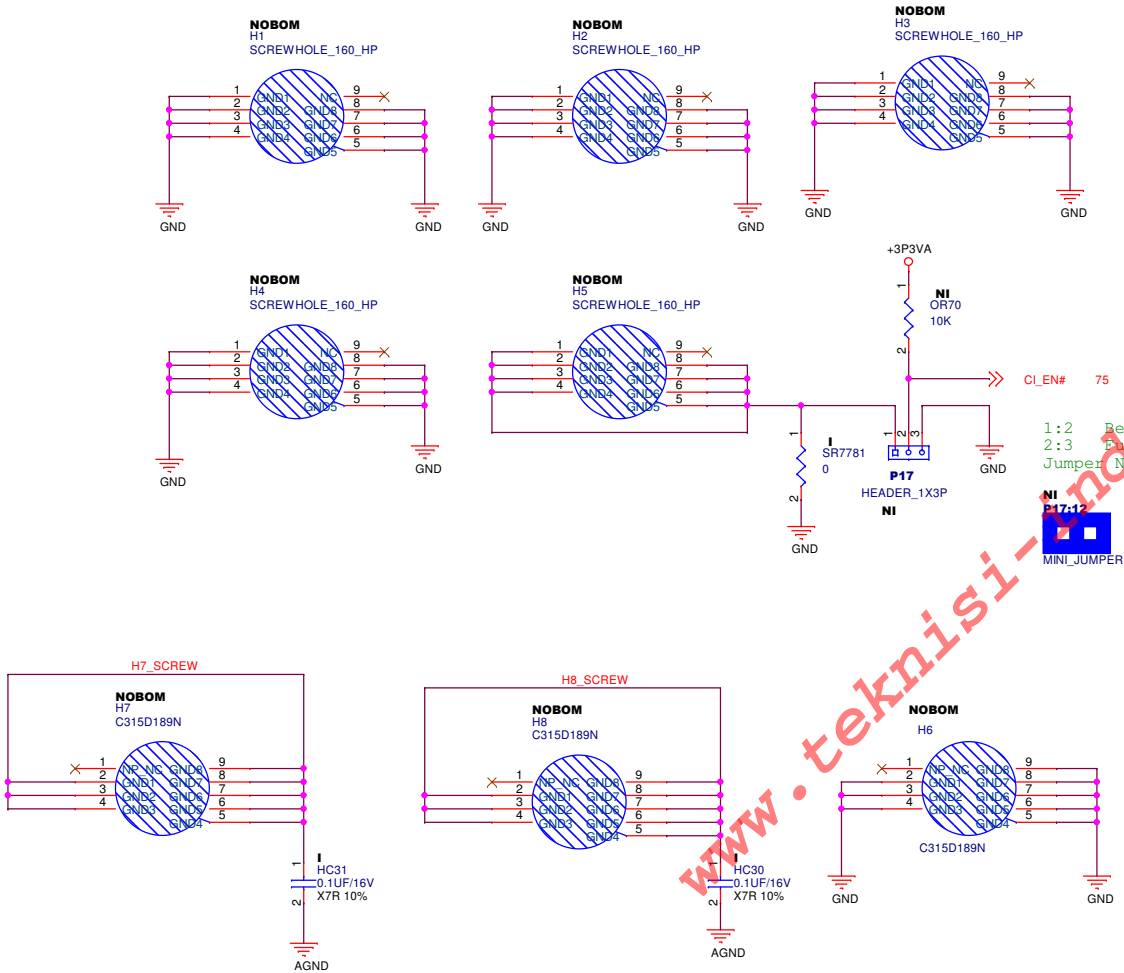
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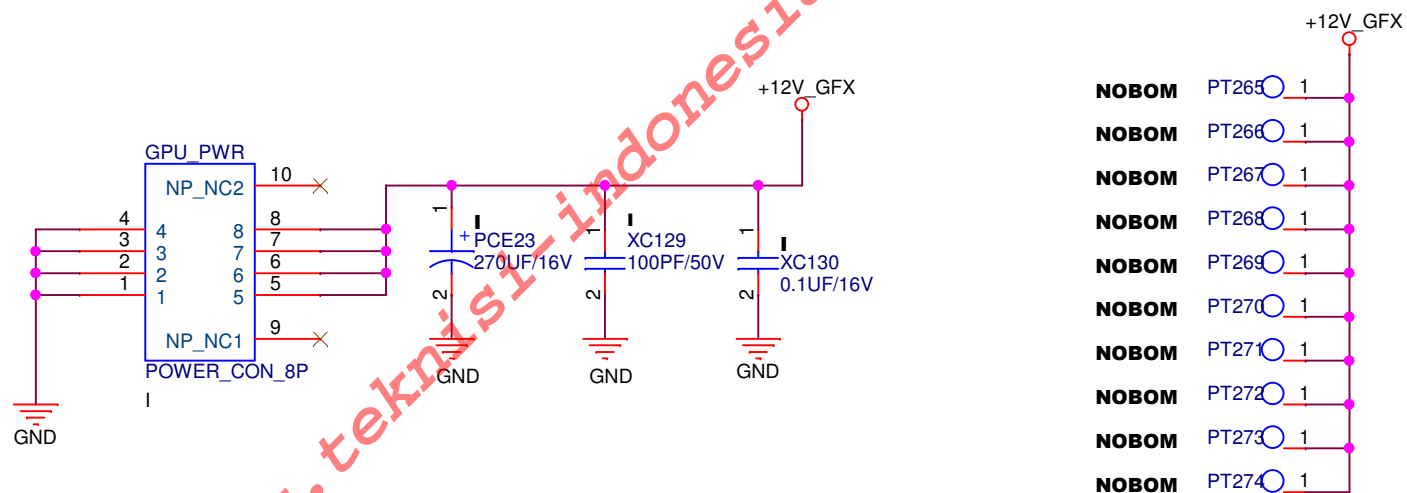
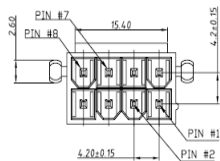
<b>PEGATRON</b>		<b>Title :</b> FAN CIRCUIT	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name		Rev
A3	IPCFL-SC		A00
Date: Monday, July 24, 2017		Sheet 71 of 82	



<Variant Name>			
<b>PEGATRON</b>		Title : TPM	
Pegatron Corp.		Engineer: Terry Wu	
Size B	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet 72 of 82	

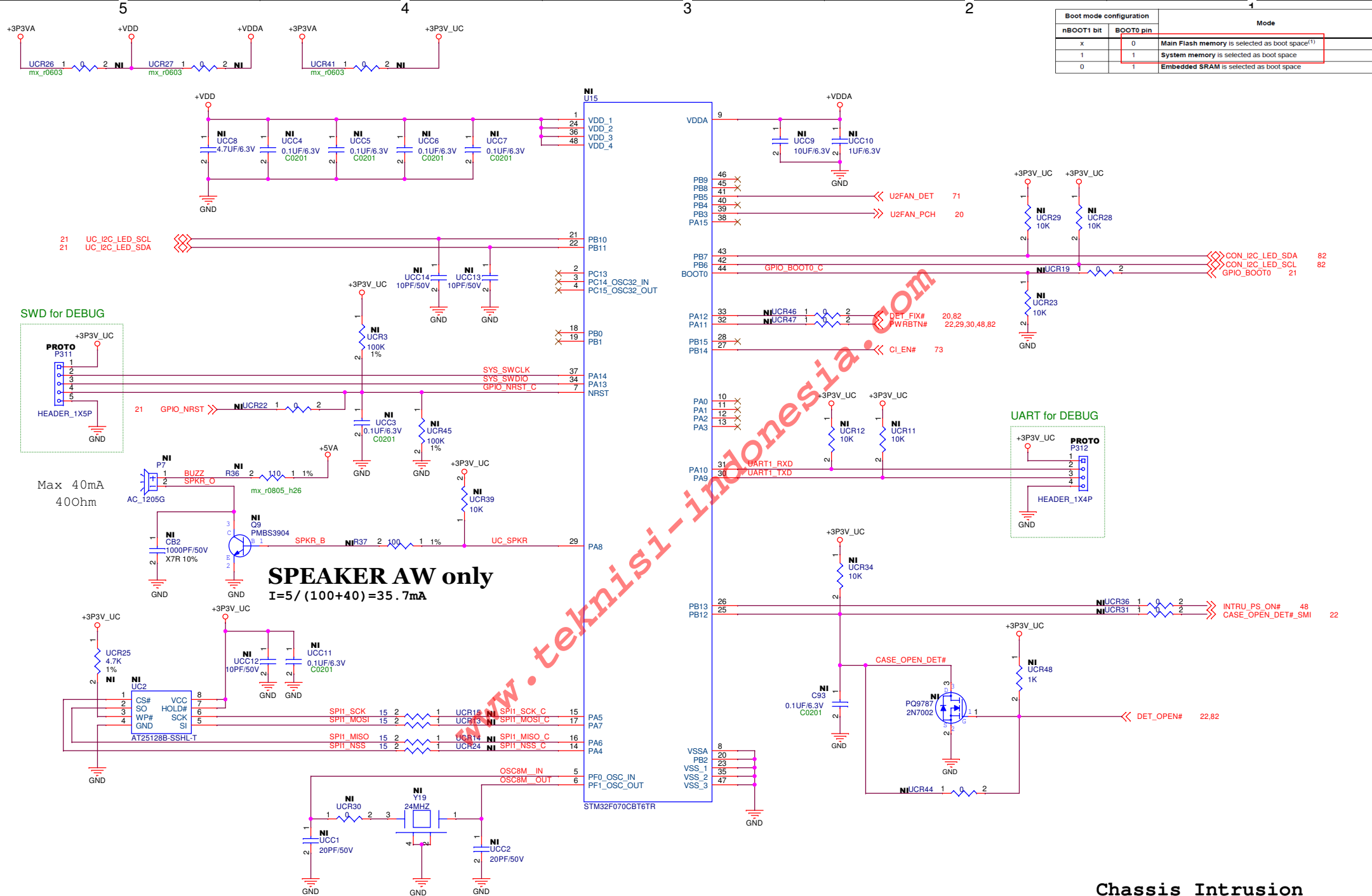






<Variant Name>

<b>PEGATRON</b>		Title : GPU_PWR	
Pegatron Corp.		Engineer: Terry Wu	
Size A	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet 74 of 82	



## Chassis Intrusion

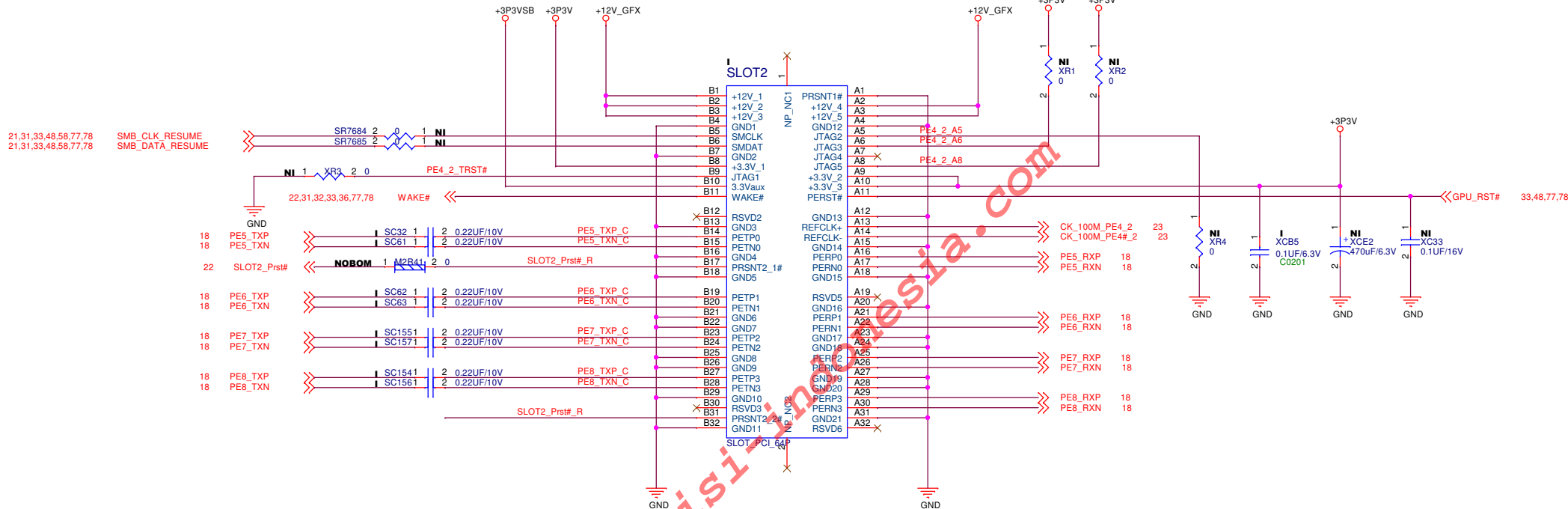
<Variant Name>

**PEGATRON** Title: **Lighting Micro-controller**

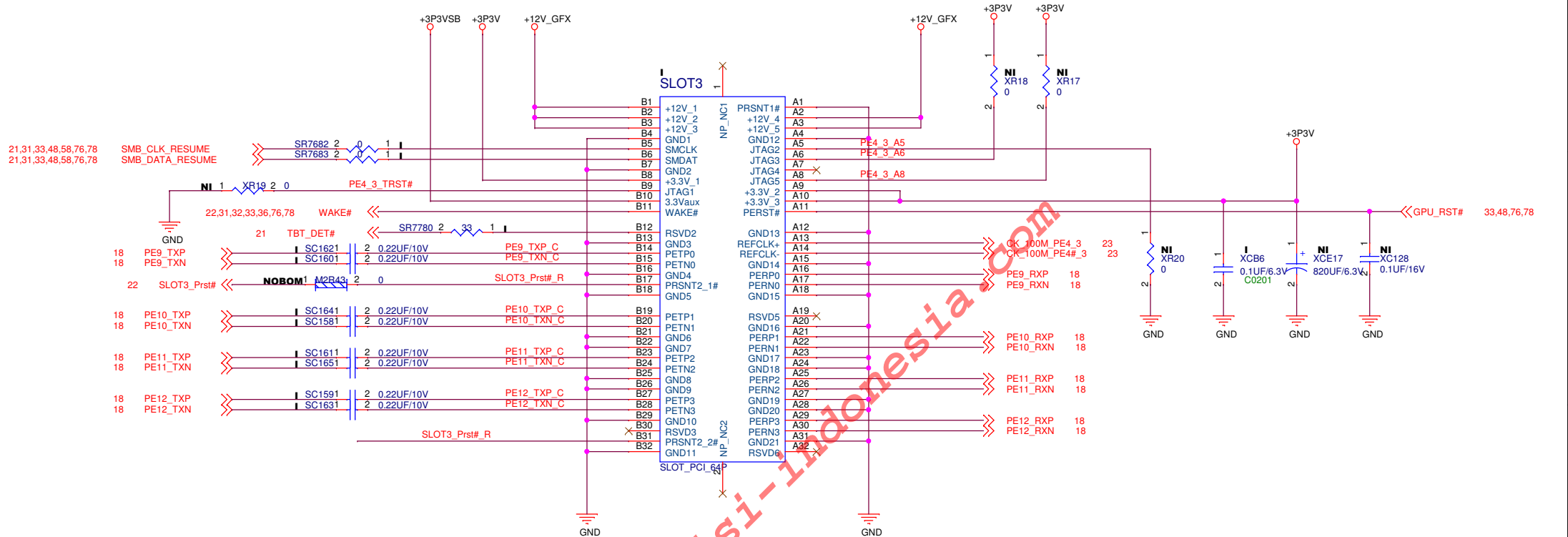
Pegatron Corp.

Engineer: **Terry Wu**

Size	Project Name	Rev
A3	IPCFL-SC	A00
Date: Monday, July 24, 2017	Sheet 75 of 82	



<Variant Name>



<Variant Name>		
<b>PEGATRON</b> Title : PCI-E X4 SLOT 3		
Pegatron Corp. Engineer: Terry Wu		
Size B	Project Name <b>IPCFL-SC</b>	Rev A00
Date: Monday, July 24, 2017		Sheet 77 of 82

Date: Monday, July 24, 2017 Sheet 78 of 82

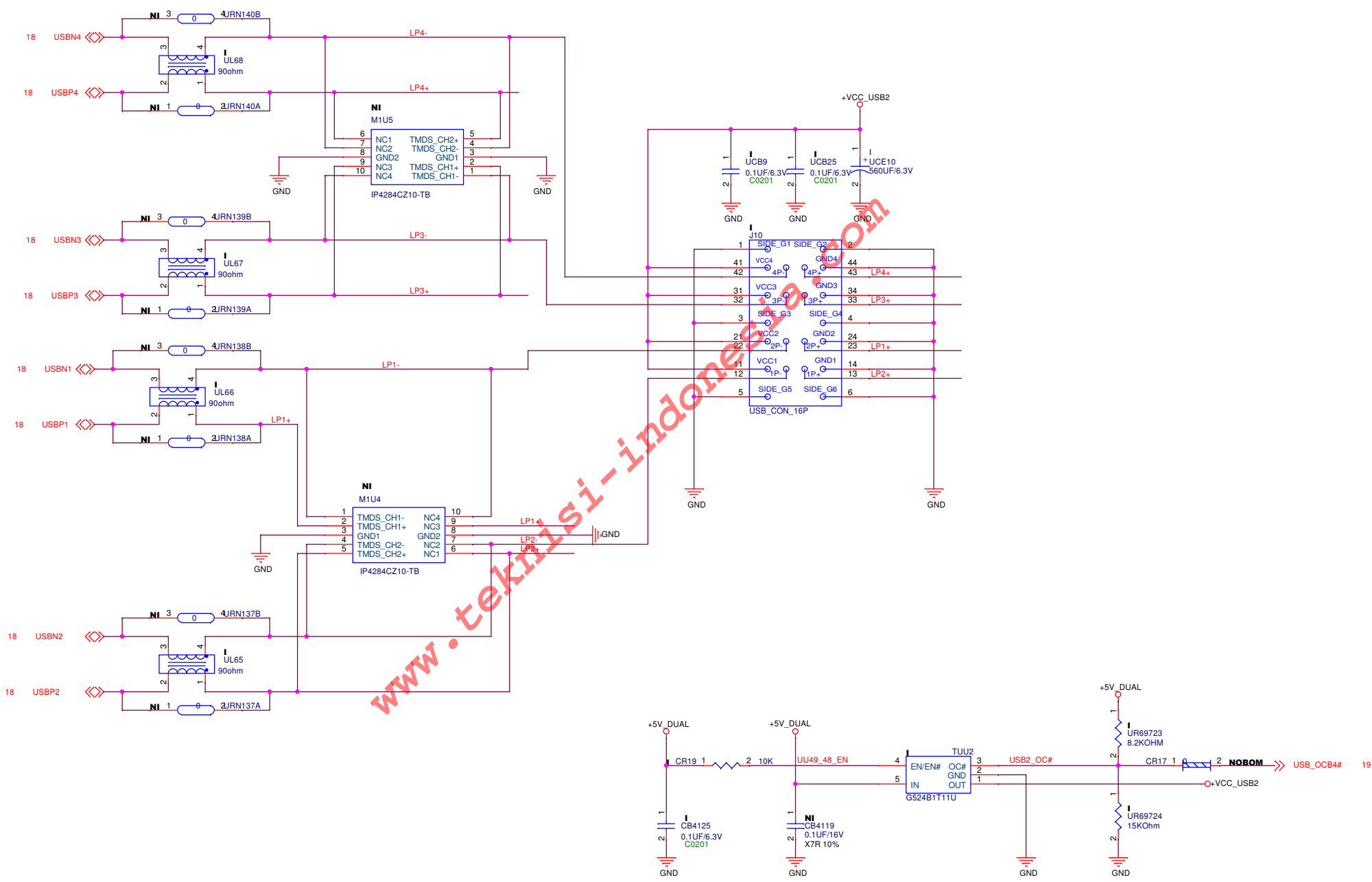
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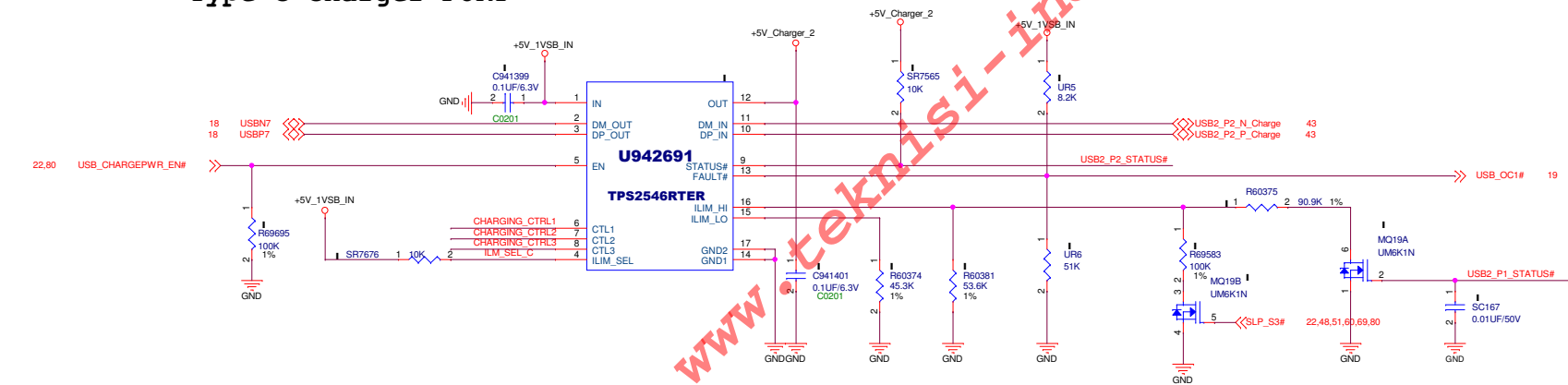
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2

1



## Type-C Charger PORT



<Variant Name>

Pegatron Corp.		Engineer: Terry Wu	
Size Custom	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet	80 of 82



